

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, MBP15

04/24/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
?		?	?	?	?

Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	(T9_MLB)	08/23/2006
3	Power Block Diagram	(T9_MLB)	08/23/2006
4	Power Block Diagram	N/A	N/A
5	BOM Configuration	N/A	N/A
6	Revision History	N/A	N/A
7	Functional / ICT Test	(MASTER)	(MASTER)
8	Power Aliases	(MASTER)	(MASTER)
9	Signal Aliases	(T9_MLB)	08/23/2006
10	CPU FSB	T9_NOME	03/16/2007
11	CPU Power & Ground	T9_NOME	03/16/2007
12	CPU Decoupling & VID	M76_MLB	03/19/2007
13	eXtended Debug Port (XDP)	T9_NOME	12/12/2006
14	NB CPU Interface	T9_NOME	03/16/2007
15	NB PEG / Video Interfaces	T9_NOME	03/16/2007
16	NB Misc Interfaces	T9_NOME	03/16/2007
17	NB DDR2 Interfaces	T9_NOME	03/16/2007
18	NB Power 1	T9_NOME	03/16/2007
19	NB Power 2	T9_NOME	03/16/2007
20	NB Grounds	T9_NOME	03/16/2007
21	NB Standard Decoupling	T9_NOME	01/17/2007
22	NB Graphics Decoupling	M76_MLB	03/12/2007
23	SB Enet, Disk, FSB, LPC	T9_NOME	03/16/2007
24	SB PCI, PCIE, DMI, USB	T9_NOME	03/16/2007
25	SB Pwr Mgt, GPIO, Clink	T9_NOME	03/16/2007
26	SB Power & Ground	T9_NOME	03/16/2007
27	SB Decoupling	T9_NOME	01/17/2007
28	SB Misc	(T9_MLB)	08/24/2006
29	Clock (CK505)	T9_NOME	03/16/2007
30	Clock Termination	(MASTER)	08/23/2006
31	DDR2 SO-DIMM Connector A	(M59_SYNC)	08/24/2006
32	DDR2 SO-DIMM Connector B	(M59_SYNC)	08/24/2006
33	Memory Active Termination	(T9_NOME)	11/14/2006
34	Left I/O Board Connector	(M59_SYNC)	08/24/2006
35	Ethernet (Yukon)	T9_NOME	03/16/2007
36	Yukon Power Control	T9_NOME	03/16/2007
37	Ethernet Connector	M76_MLB	03/19/2007
38	FireWire Link (TSB83AA22)	M76_MLB	03/19/2007
39	FireWire PHY (TSB83AA22)	M76_MLB	03/19/2007
40	FireWire Port Power	M76_MLB	03/19/2007
41	FireWire Ports	M76_MLB	03/19/2007
42	PATA Connector	(MASTER)	(MASTER)
43	External USB Connector	M76_MLB	03/19/2007
44	Left Clutch Barrel Interconnect	M76_MLB	03/19/2007

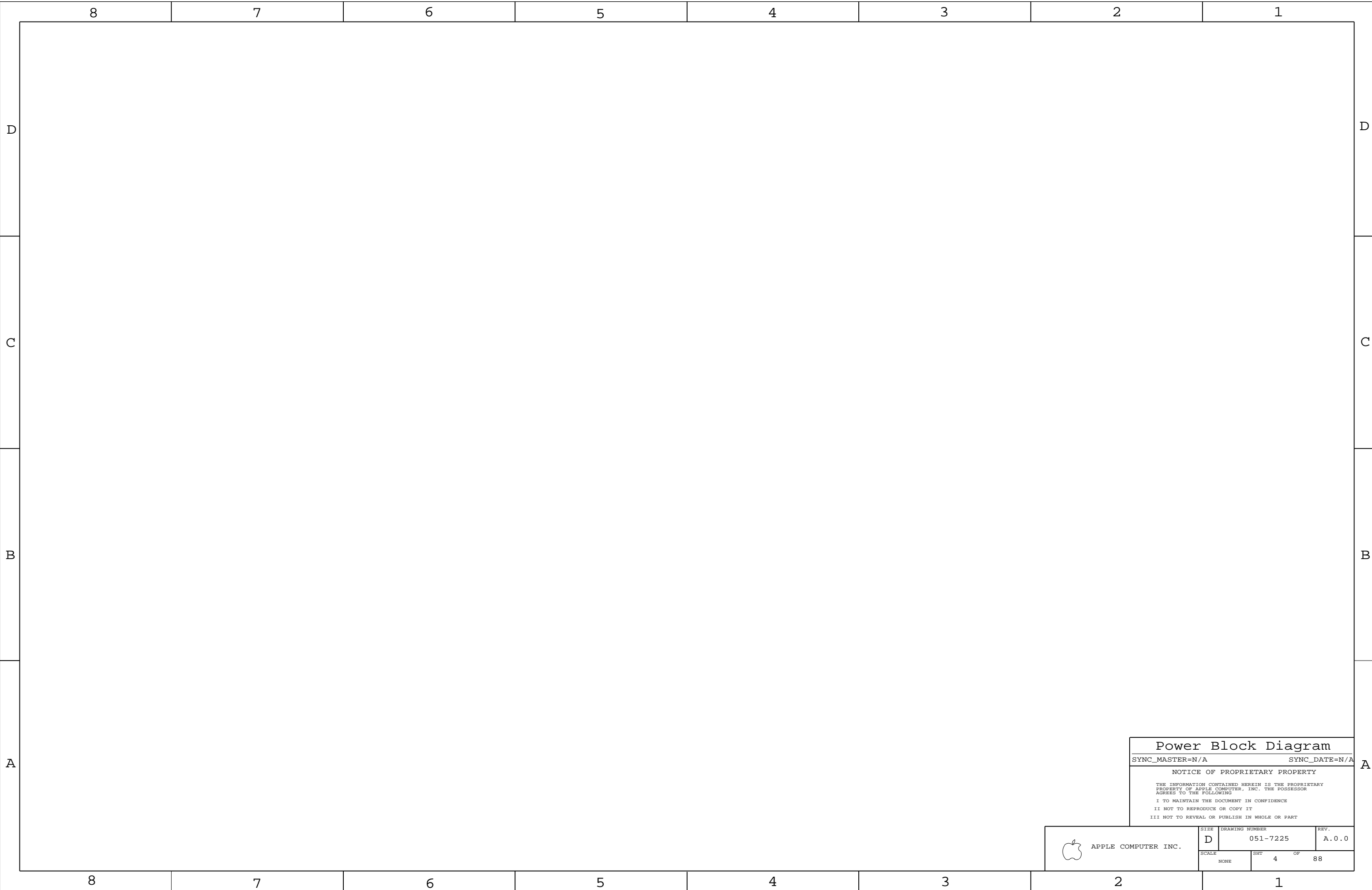
Page	Contents	Sync	Date
45	SMC	T9_NOME	01/17/2007
46	SMC Support	(MASTER)	(MASTER)
47	LPC+ Debug Connector	M76_MLB	03/19/2007
48	SMBus Connections	(MASTER)	(MASTER)
49	Current & Voltage Sensing	(MASTER)	(MASTER)
50	Current Sensing	(MASTER)	(MASTER)
51	Thermal Sensors	(MASTER)	(MASTER)
52	Fan Connectors	M76_MLB	03/19/2007
53	ALS Support	M76_MLB	03/19/2007
54	Sudden Motion Sensor (SMS)	M76_MLB	03/19/2007
55	SPI BootROM	T9_NOME	03/16/2007
56	PBus-In & Battery Connectors	(M59_SYNC)	09/09/2006
57	Power FETs	M76_MLB	03/19/2007
58	IMVP6 CPU VCore Regulator	M76_MLB	01/23/2007
59	IMVP6 NB Gfx Core Regulator	M76_MLB	03/19/2007
60	5V / 3.3V Power Supply	M76_MLB	03/19/2007
61	1.25V / 1.05V Power Supply	M76_MLB	03/12/2007
62	1.8V DDR2 Supply	M76_MLB	03/19/2007
63	1.5V Power Supply	M76_MLB	03/12/2007
64	FW PHY Power Supplies	M76_MLB	03/19/2007
65	3.425V G3Hot Supply & Power Control	(MASTER)	(MASTER)
66	NV G84M PCI-E	(MASTER)	(MASTER)
67	NV G84M Core/FB Power	(MASTER)	(MASTER)
68	NV G84M Frame Buffer I/F	(MASTER)	(MASTER)
69	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
70	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
71	NV G84M GPIO/MIO/Misc	(MASTER)	(MASTER)
72	GPU Straps	(MASTER)	(MASTER)
73	NV G84M Video Interfaces	(MASTER)	(MASTER)
74	GPU (G84M) Core Supply	(MASTER)	(MASTER)
75	LVDS Display Connector	(MASTER)	(MASTER)
76	DVI Display Connector	(MASTER)	(MASTER)
77	LVDS Interface Mux	(MASTER)	(MASTER)
78	Project Specific Connectors	(M59_SYNC)	08/24/2006
79	CPU/FSB Constraints	T9_NOME	01/17/2007
80	NB Constraints	T9_NOME	01/17/2007
81	Memory Constraints	T9_NOME	01/17/2007
82	SB Constraints (1 of 2)	T9_NOME	01/17/2007
83	SB Constraints (2 of 2)	T9_NOME	01/17/2007
84	Clock & SMC Constraints	T9_NOME	01/17/2007
85	FireWire Constraints	T9_NOME	01/17/2007
86	GPU (G84M) Constraints	(MASTER)	(MASTER)
87	Project Specific Constraints	(MASTER)	(MASTER)
88	PCB Rule Definitions	(MASTER)	(MASTER)

Schematic / PCB #'s


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7225	1	SCHEM,MLB,MBP15	SCH	CRITICAL	
820-2101	1	PCBF,MLB,MBP15	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 24 17:23:54 2007

DIMENSIONS ARE IN MILLIMETERS		METRIC		<div><div></div>Apple Computer Inc.</div>	
XX : _____					
X.XX : _____		DRAWER		NOTICE OF PROPRIETARY PROPERTY	
X.XXX : _____		DESIGN CK		THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
ANGLES : _____		ENG APPD		I TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
DO NOT SCALE DRAWING		MFG APPD		I NOT TO REPRODUCE OR COPY IT	
		QA APPD		I NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
		DESIGNER		TITLE	
		RELEASE		SCHEM , MLB , MBP15	
		SCALE			
		NONE			
<div><div></div></div>		MATERIAL/FINISH		DRAWING NUMBER	
THIRD ANGLE PROJECTION		NOTED AS		051-7225	
		APPLICABLE		REV. A.0.0	
		SIZE		SHT 1 OF 88	
		D			



Power Block Diagram		
SYNC_MASTER=N/A		SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 4 OF 88	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA, 2.2GHZ, 128SAM_VRAM, M75, MBP15	M75_COMMON, EEE_X5D, CPU_2_2GHZ, FB_128_SAMSUNG
630-7932	PCBA, 2.4GHZ, 256SAM_VRAM, M75, MBP15	M75_COMMON, EEE_X5E, CPU_2_4GHZ, FB_256_SAMSUNG
630-8659	PCBA, 2.2GHZ, 128HY_VRAM, M75, MBP15	M75_COMMON, EEE_XXS, CPU_2_2GHZ, FB_128_HYNIX
630-8662	PCBA, 2.4GHZ, 256HY_VRAM, M75, MBP15	M75_COMMON, EEE_XXT, CPU_2_4GHZ, FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128, VRAM_SAMSUNG, VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128, VRAM_HYNIX, VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3464	1	IC,MDC,SR,E1,PRQ,2.2Q,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3465	1	IC,MDC,SR,E1,PRQ,2.4Q,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,CQ,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,1P	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIM,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,1W PWR CLK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	SAE alt to TDR/SI-Tech magnetic
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Nurata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A	SYNC_DATE=N/A
-----------------	---------------

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN



APPLE COMPUTER INC.

SIZE

D

G NUMBER

051-7225

REV.

A.O.C

SCAL

NONE

SHT

OF

	8	7	6	5	4	3	2	1
	<div><div>PROTO</div><div>See Perforce change notes for updates before Proto Release 12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)</div><div>EVT</div><div>8.1.0: 01/05/07 -- Clock Termination: Removed NO STUFF property from R3067 01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ) 8.2.0: 01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs) 9.0.0: 01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap) 01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements) 01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76 9.1.0: 01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0 01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K 01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support 01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs 01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable 01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request 01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131 01/17/07 -- BOM: Added Hynix BOM configurations 9.2.0: 01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B 01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms 01/18/07 -- IMVP: Updated BOMPTIONs and values for ISL9504B 01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP 01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap) 9.3.0: 01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB 01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x 01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101 01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails 01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path 9.4.0: 01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible 01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787) 9.5.0: 01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998) 01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975) 01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility 01/22/07 -- BOM: Added BOMPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup) 01/22/07 -- BOM: Selected PlV8S3_lV825 BOMOPTION to lift voltage at FB memories 10.0.0: 01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248) 01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMPTIONs to GPU straps) 01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)</div><div><div>EVT_SE</div><div>10.1.0: 01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0 01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings 01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes 10.2.0: 01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST 01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes 11.0.0: 01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K) 01/25/07 -- BOM: Updated all Intel APNs to use QS parts 01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03) 12.0.0: 02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup 02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup 02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain 02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain 02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)</div><div>DVT</div><div>12.1.0: 02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm) 02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K) 02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435) 02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927) 02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported) 02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453) 02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates 02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773) 12.2.0: 02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378) 02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462) 12.3.0: 02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating) 02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109) 02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109) 03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF) 03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines 12.4.0: 03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882) 03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272) 12.5.0: 03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements 12.6.0: 03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on) 03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height 12.7.0: 03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity 03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request 03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO) 03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage</div></div></div>							
	8	7	6	5	4	3	2	1

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
15.0.0:
03/30/07 -- SIL: Changed R5031 to 2.21K and R5032 to 9.53K to raise SIL current approx 15% (lightpipe dimmed by 20%)
03/30/07 -- Power Supply: Changed 1.05V power supply current limit to 10A from 8A (R7455 to 5.62k -- rdar://5095642)
04/03/07 -- Power Supply: Changed numerous 10K Rs to 100K for Energy Star compliance (rdar://5102118)
04/03/07 -- GPU FB: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN
04/03/07 -- CPU Vcore: Changed R7117,C7134 and R7115,R7130 for calibration improvements (rdar://5085959)
04/03/07 -- Released for DVT (BOM update)
16.0.0:
04/17/07 -- Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive S5 enable pins directly
04/17/07 -- Released for DVT (As-Built)

PVT

16.1.0:
04/18/07 -- GPU Misc: Added R8735-37 to implement PCI DEVID 0x407 in hardware
16.2.0:
04/18/07 -- Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)
04/18/07 -- Modules: Updated Intel chipset to PRQ parts
16.3.0:
04/20/07 -- Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS
04/20/07 -- Power FETs: Changed C7095/C7083 to 16V for proper rating of parts tied to PBUS
04/20/07 -- CPU VCore: Changed C7196 to 16V to eliminate a BOM item
17.0.0:
04/20/07 -- No changes. Weekly BOM release.
A.0.0:
04/24/07 -- SB Decoupling: Changed L2700 from 155S0152 to 155S0333 for AVL updates
04/24/07 -- SMC Support: Changed R5031 to 2.37K, R5032 to 9.09K to meet SIL brightness targets
04/24/07 -- Released for PVT

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

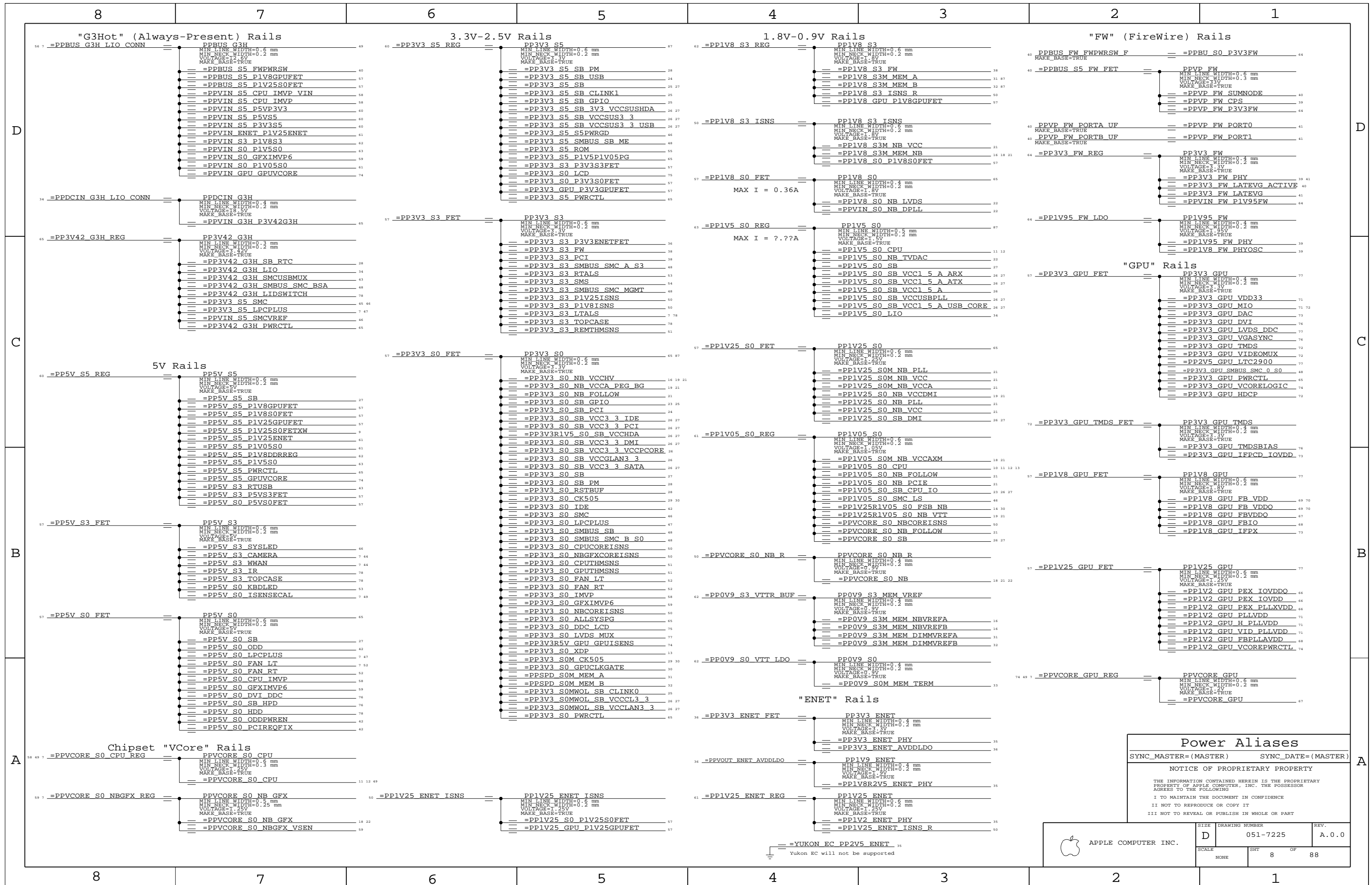
NONE

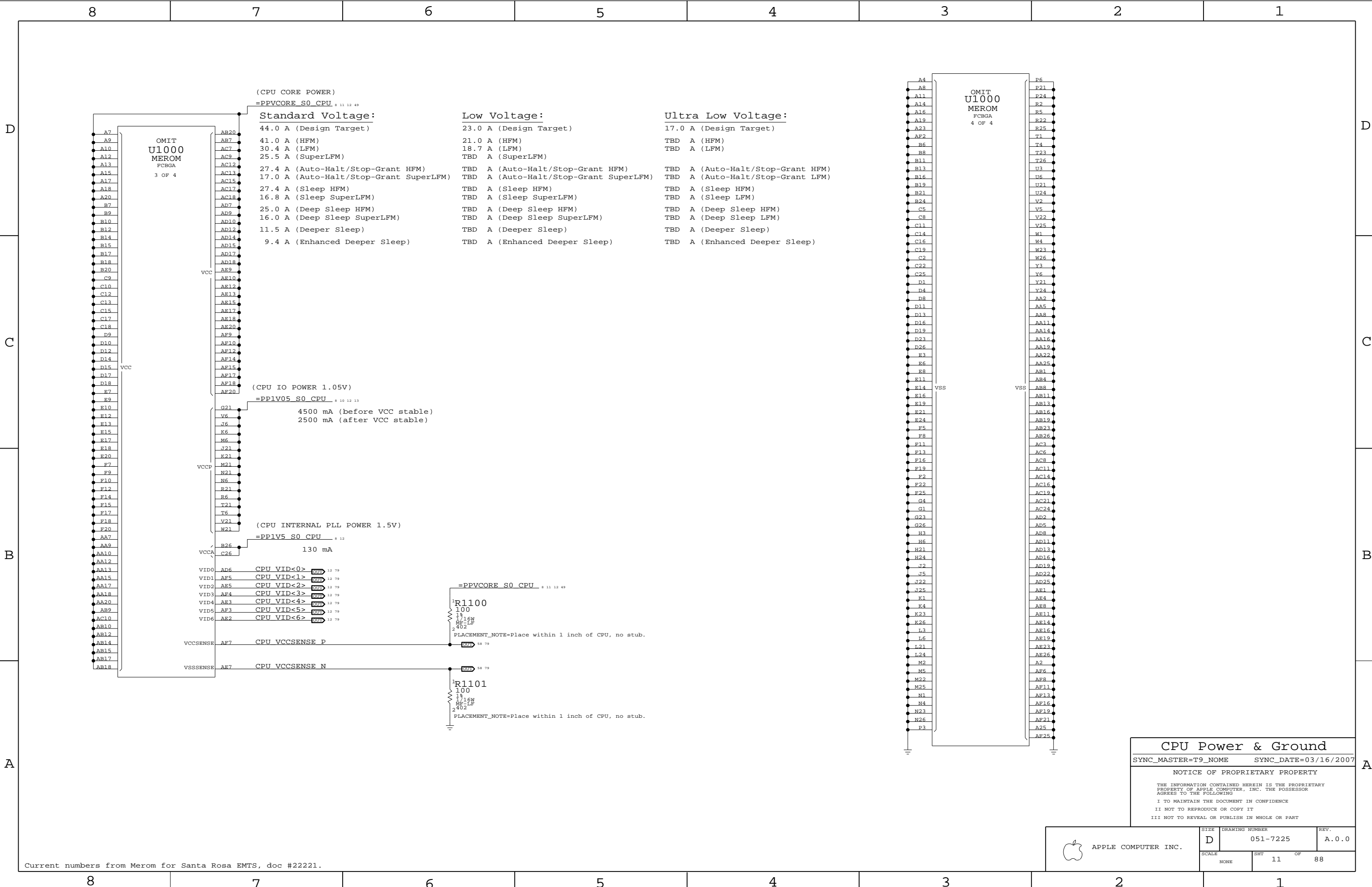
SHT

6

OF

88





CPU Power & Ground

SYNC_MASTER=T9_NOME

SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		11	88

D

C

B



C

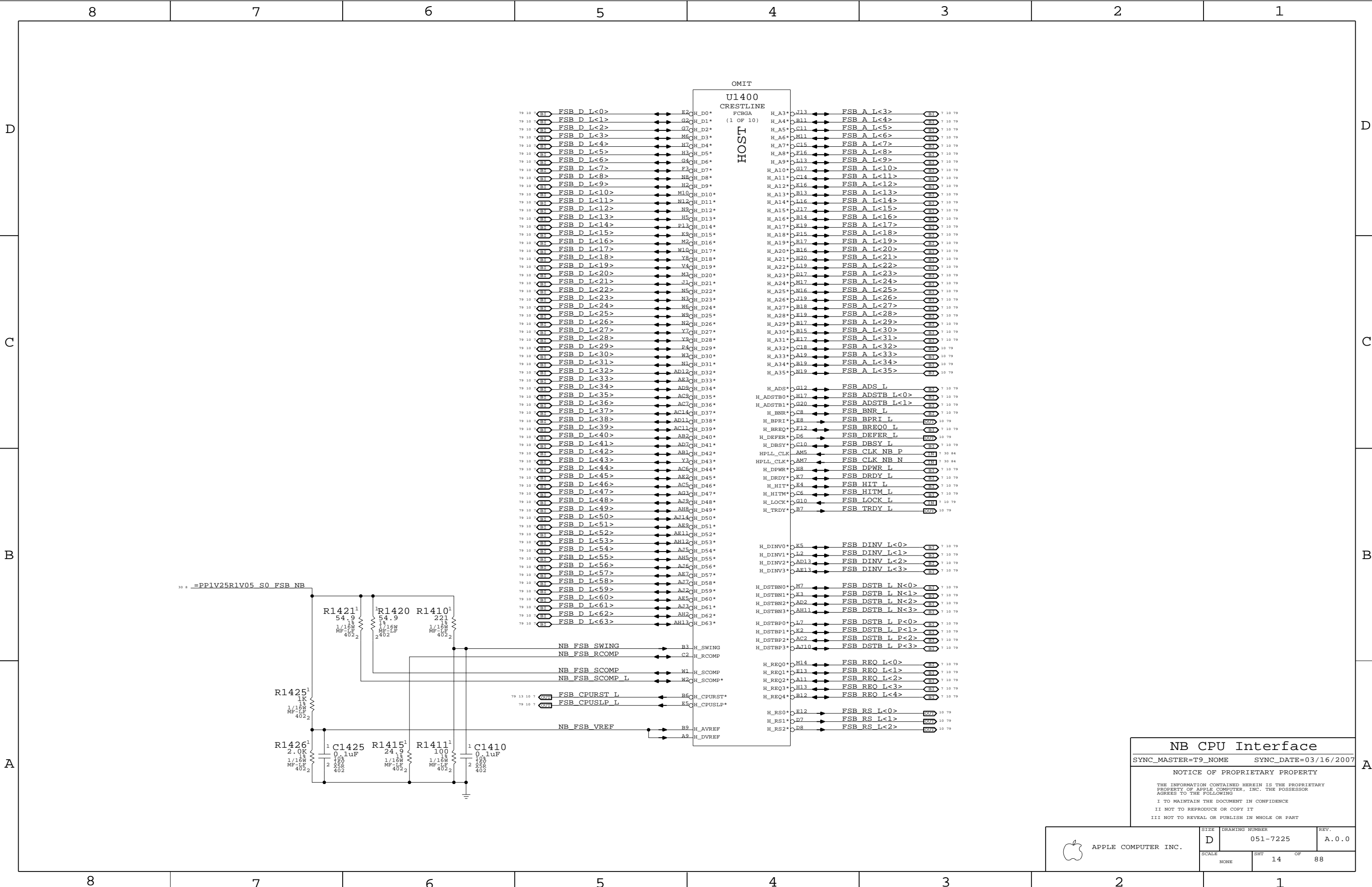
B

A

A



SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
SCALE NONE	SHT 13	OF 88



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		14	88

D

C

B

A

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

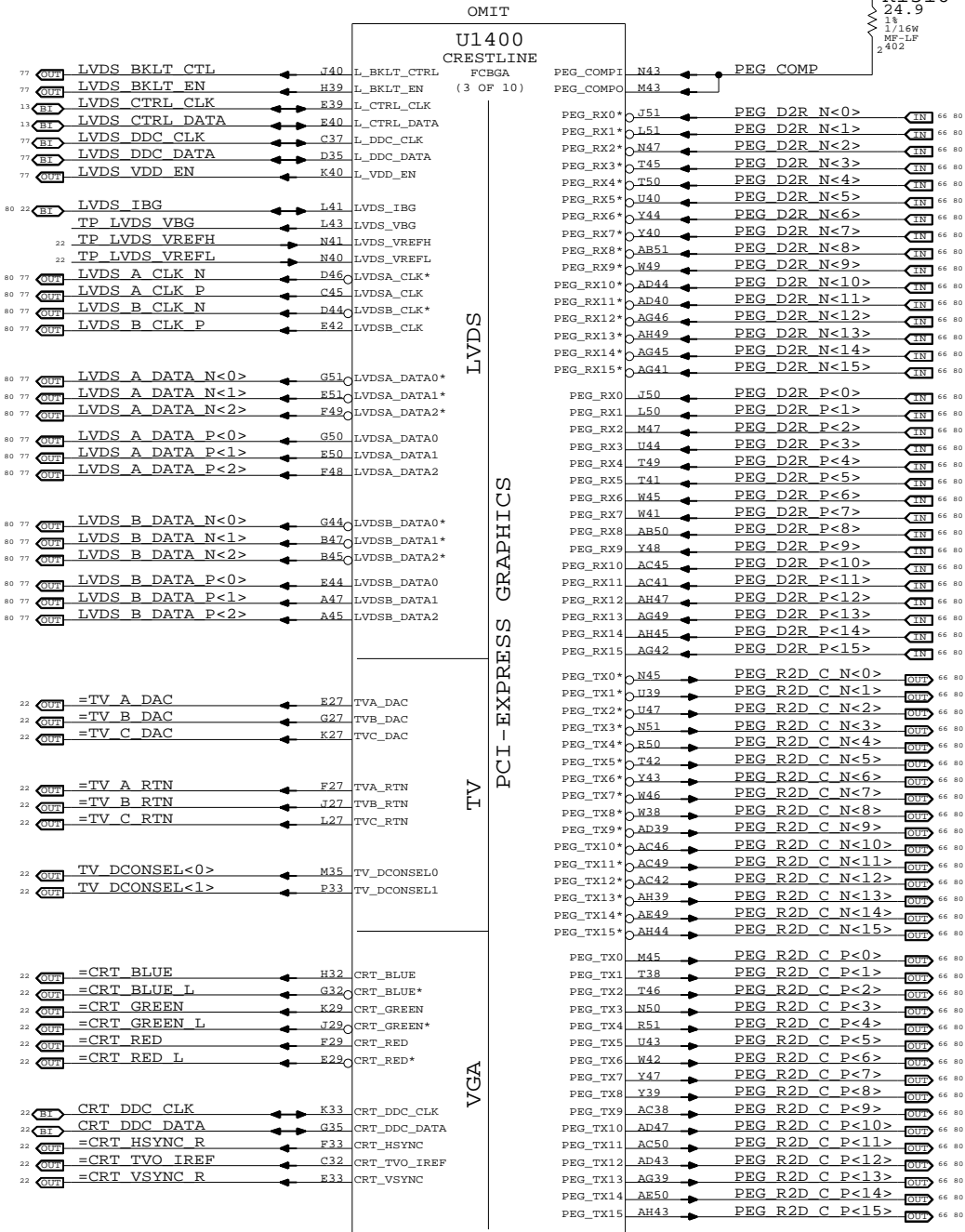
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

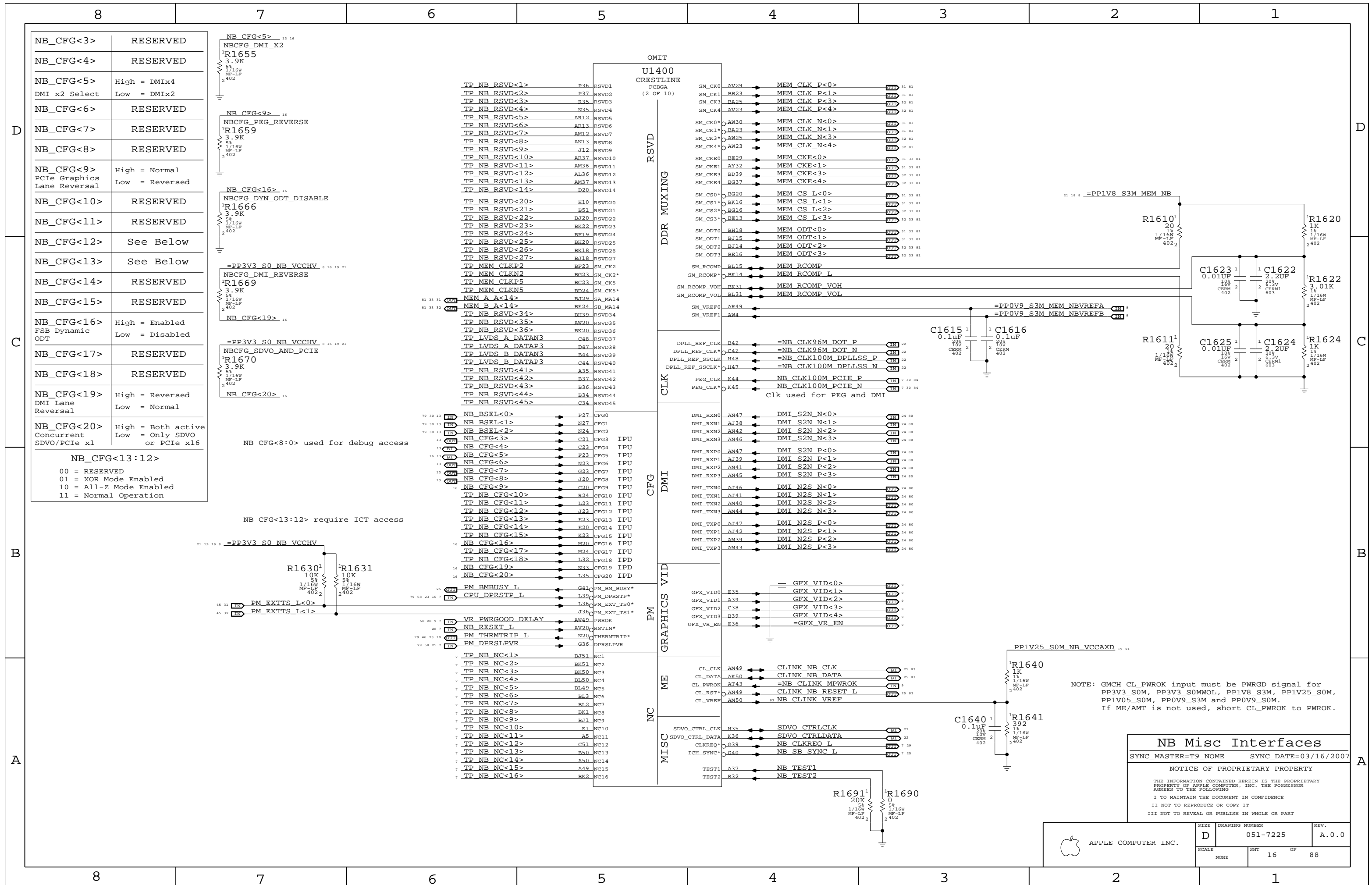
NONE

SHT

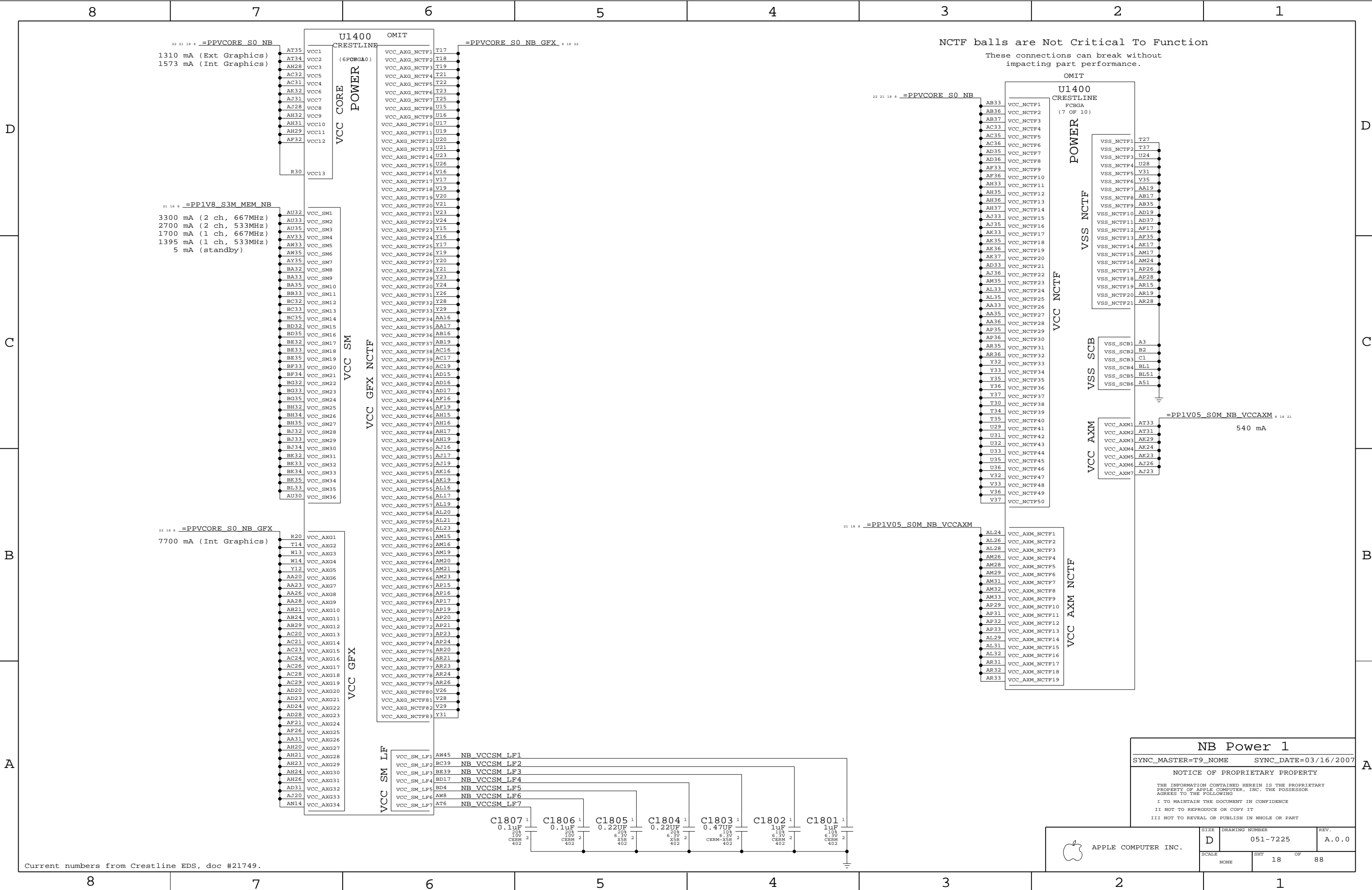
15

OF

88




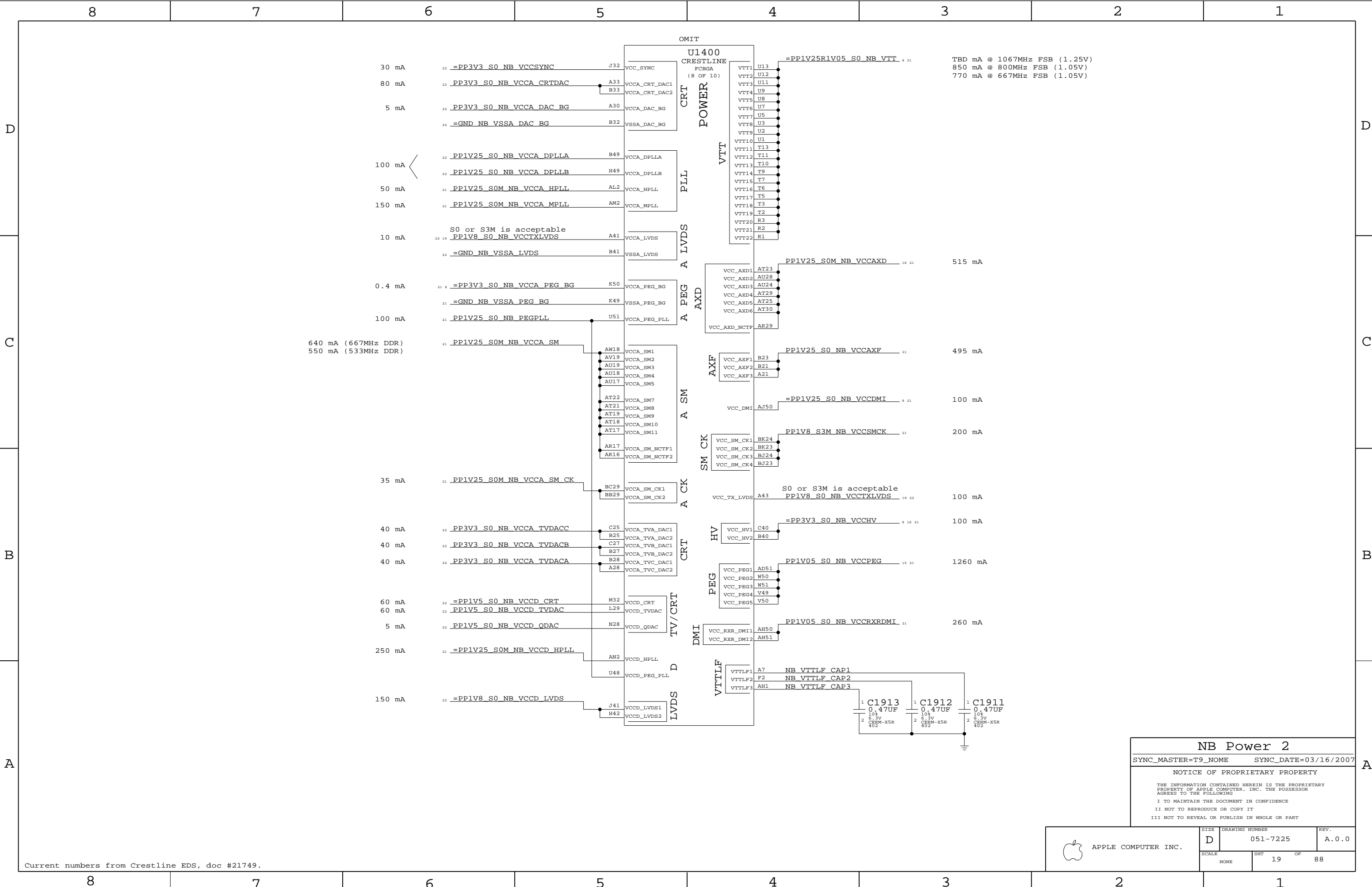




Current numbers from Crestline EDS, doc #21749.

NB Power 1		
SYNC_MASTER=T9_NOME		SYNC_DATE=03/16/2007
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 18	OF 88



NB Power 2

SYNC_MASTER=T9_NOME

SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

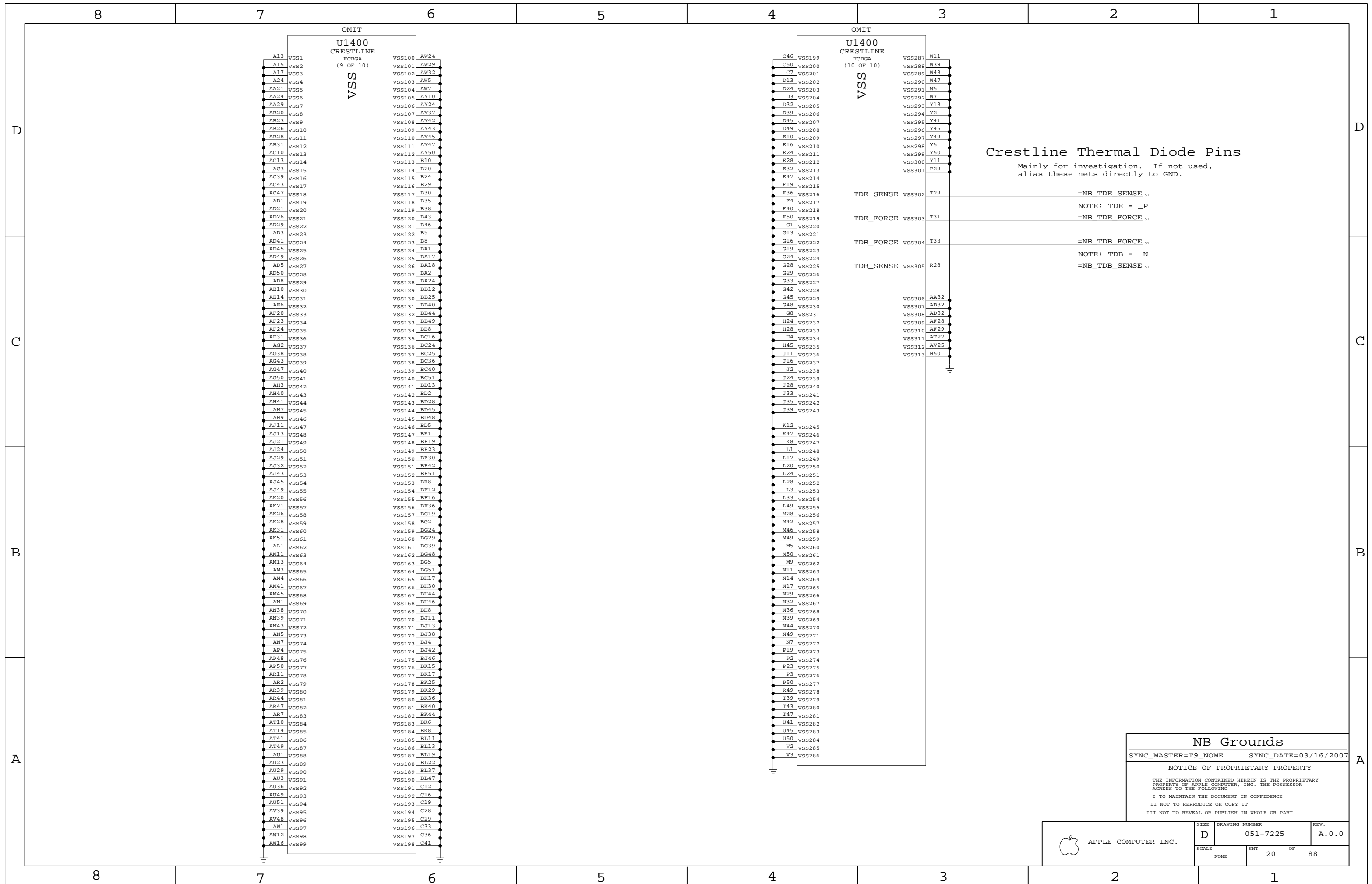
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

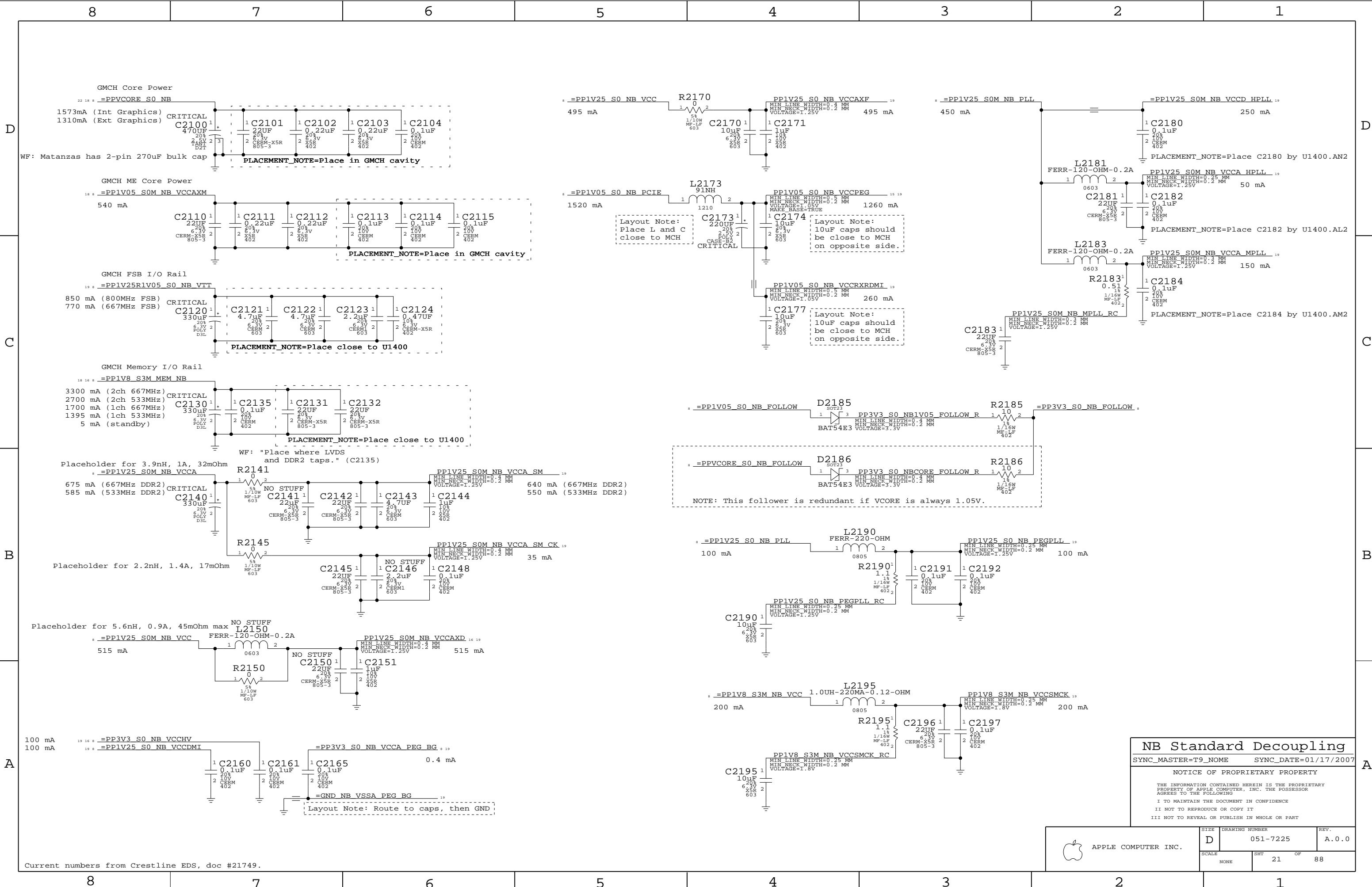
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		19	88





NB Standard Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

NOTICE OF PROPRIETARY PROPERTY

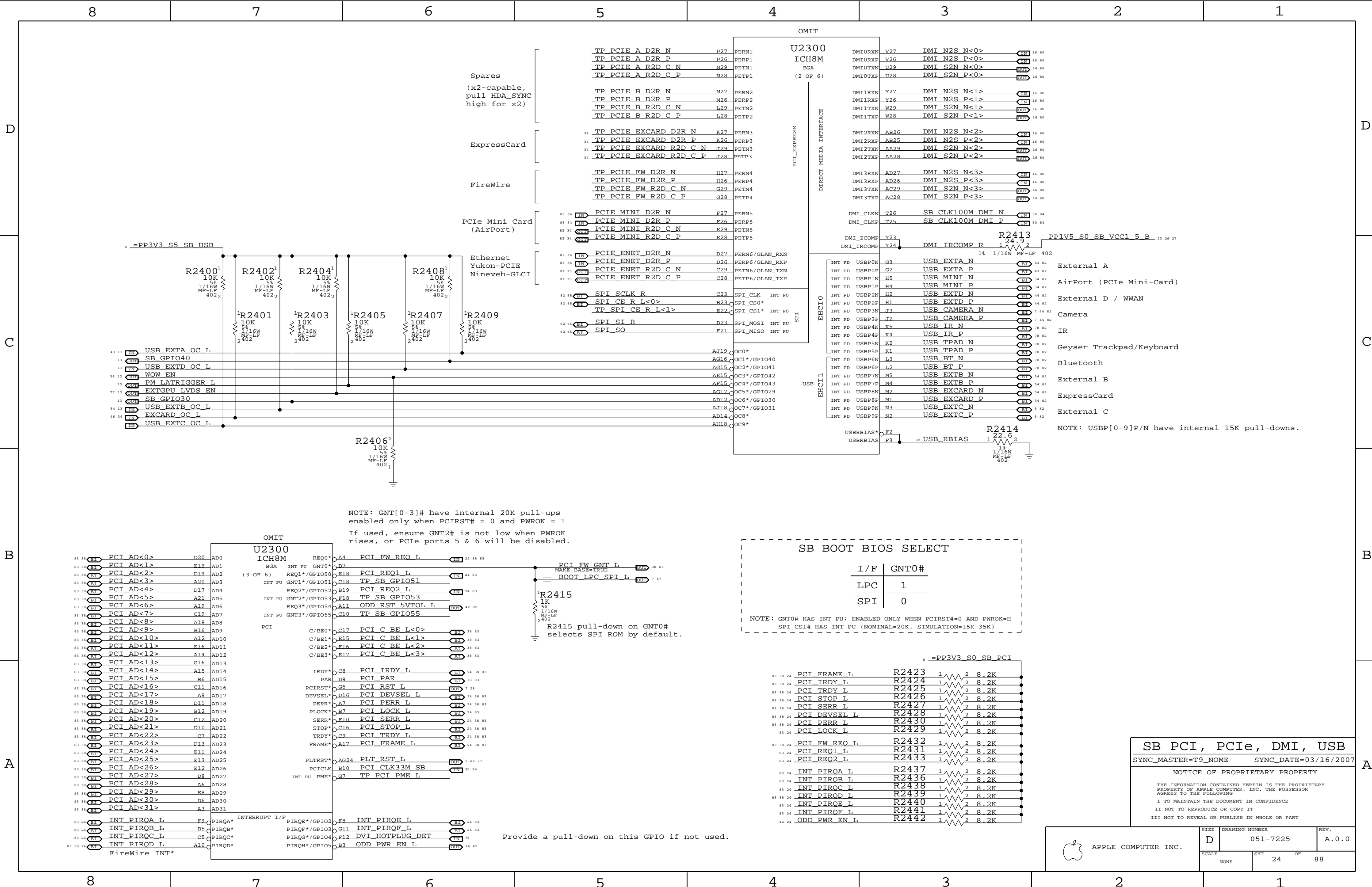
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE D	DRAWING NUMBER 051-7225		REV. A.0.0
	SCALE NONE	SHT 21	OF 88

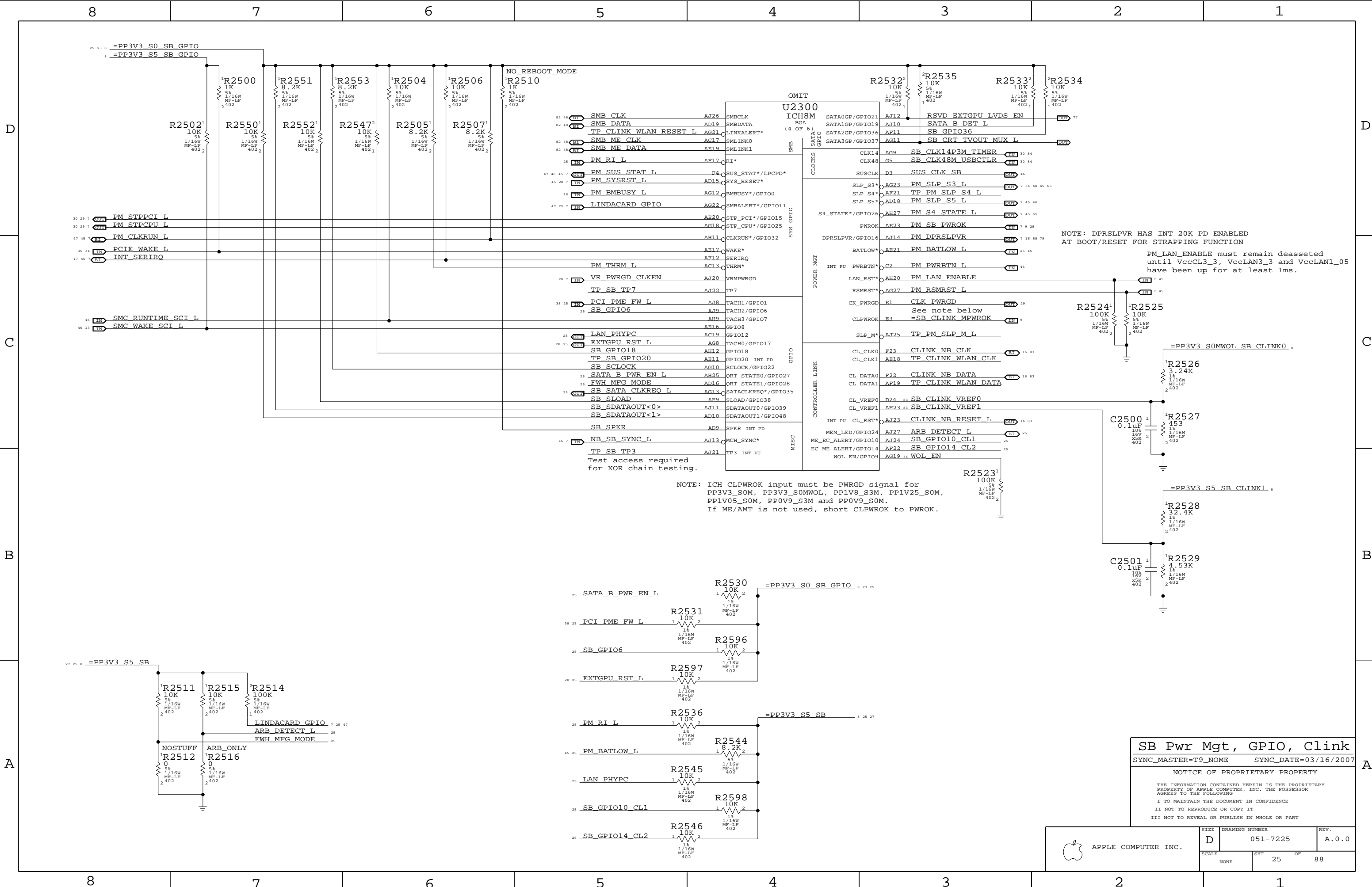


NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1

If used, ensure GNT2# is not low when PWROK rises, or PCIE ports 5 & 6 will be disabled.

NOTE: USBP[0-9]P/N have internal 15K pull-downs.

Provide a pull-down on this GPIO if not used.



SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

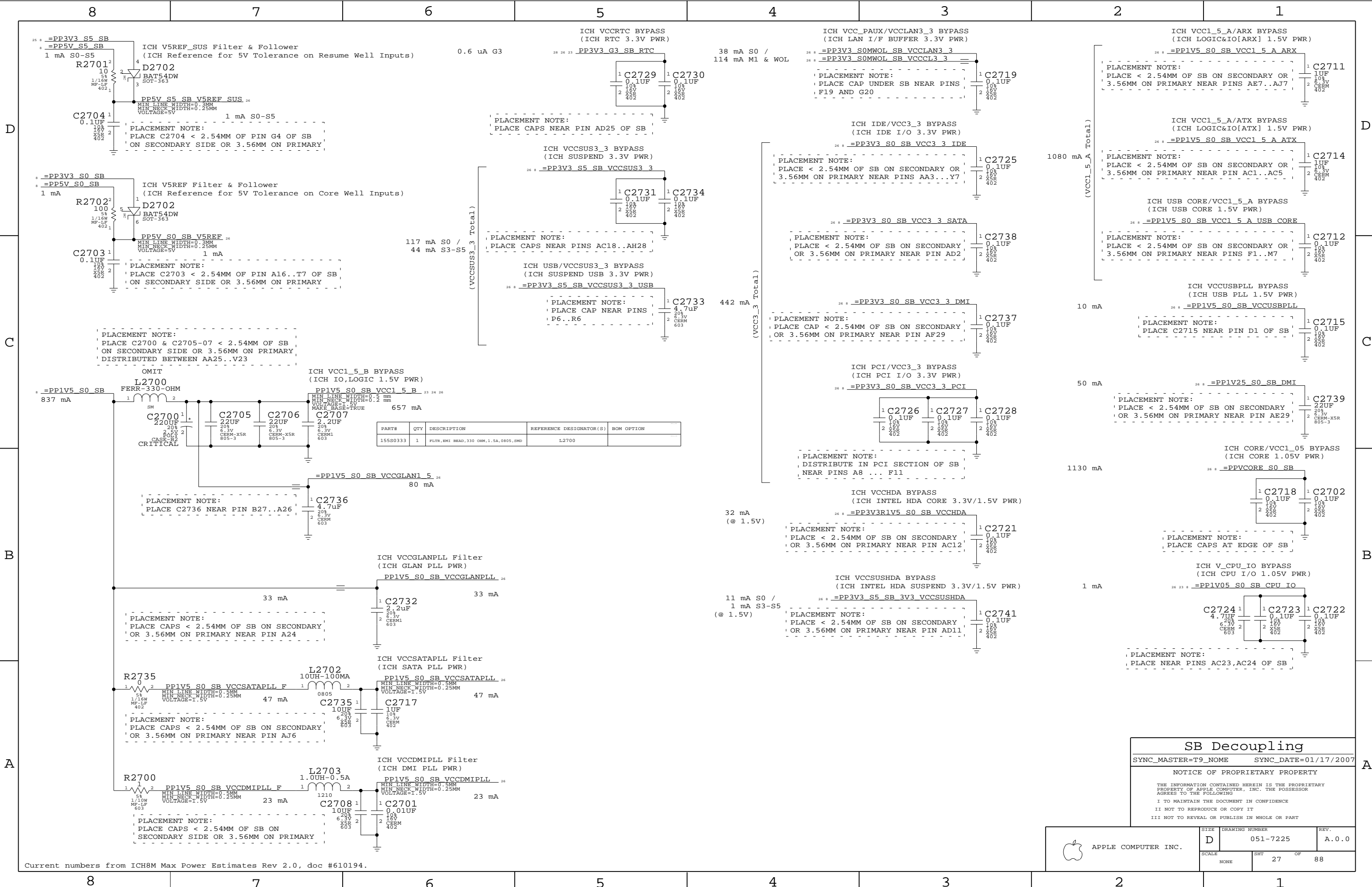
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

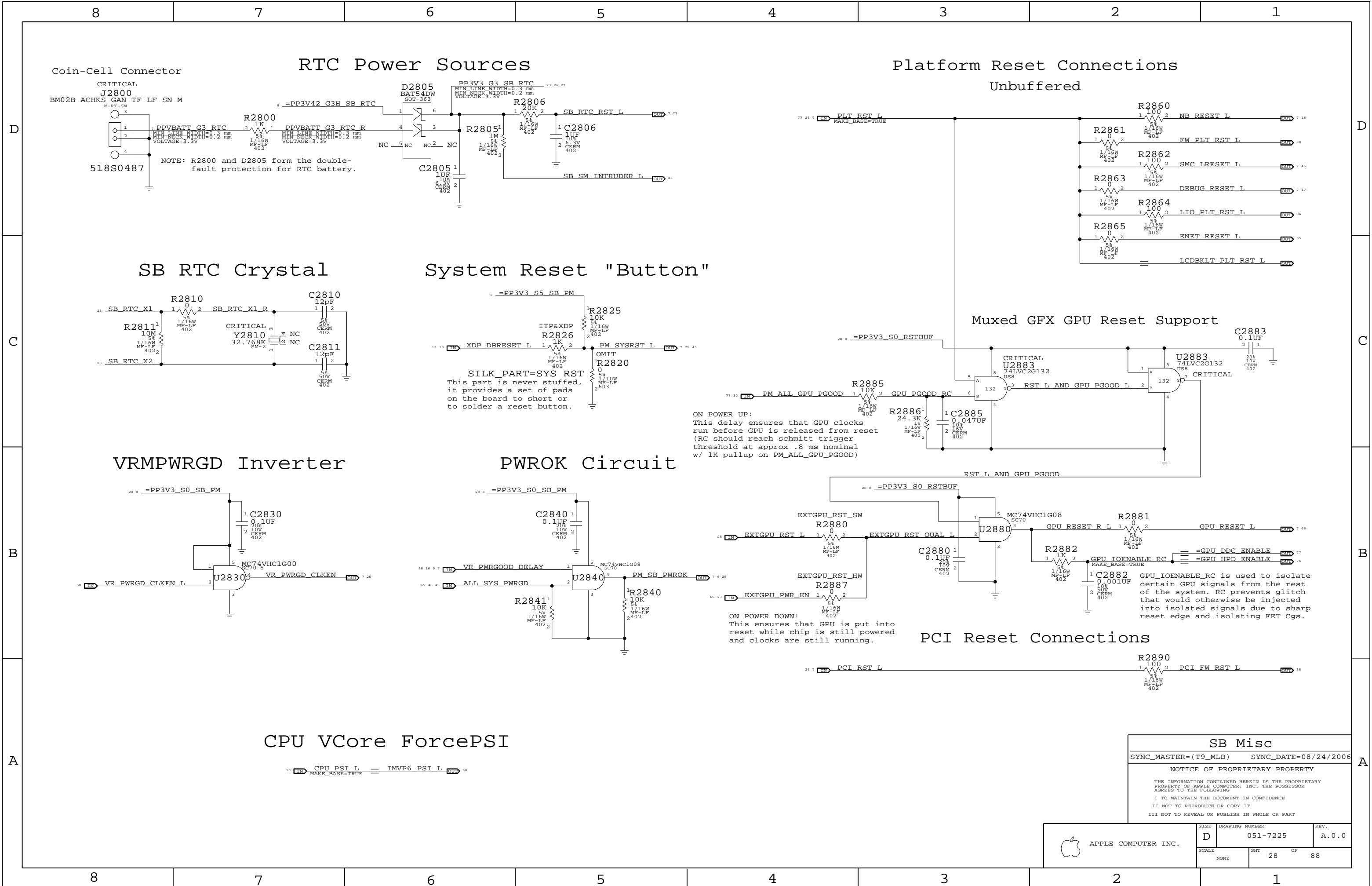
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

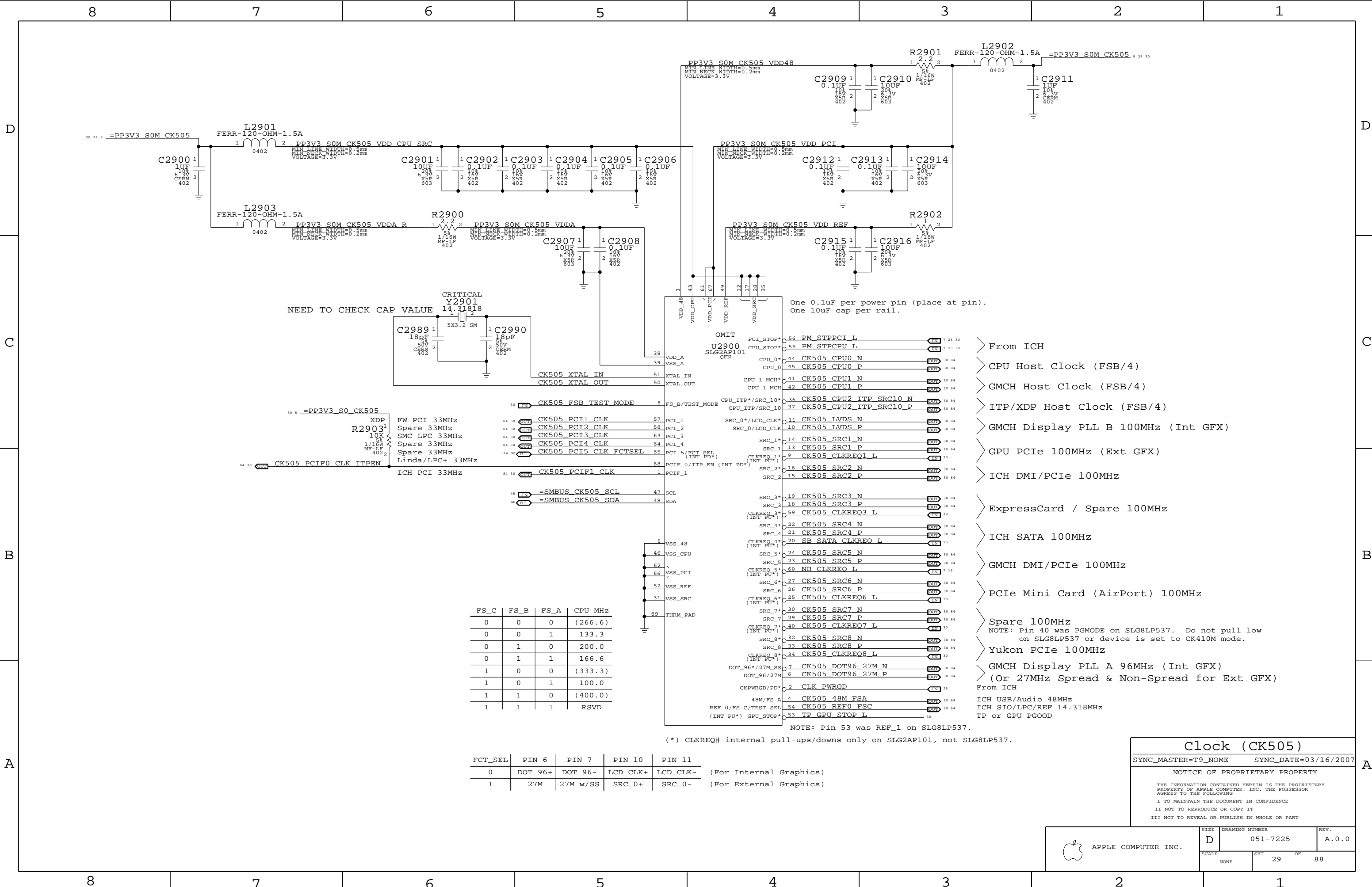
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		25	88







NEED TO CHECK CAP VALUE

One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

NONE

SHT

29

OF

88

D

C

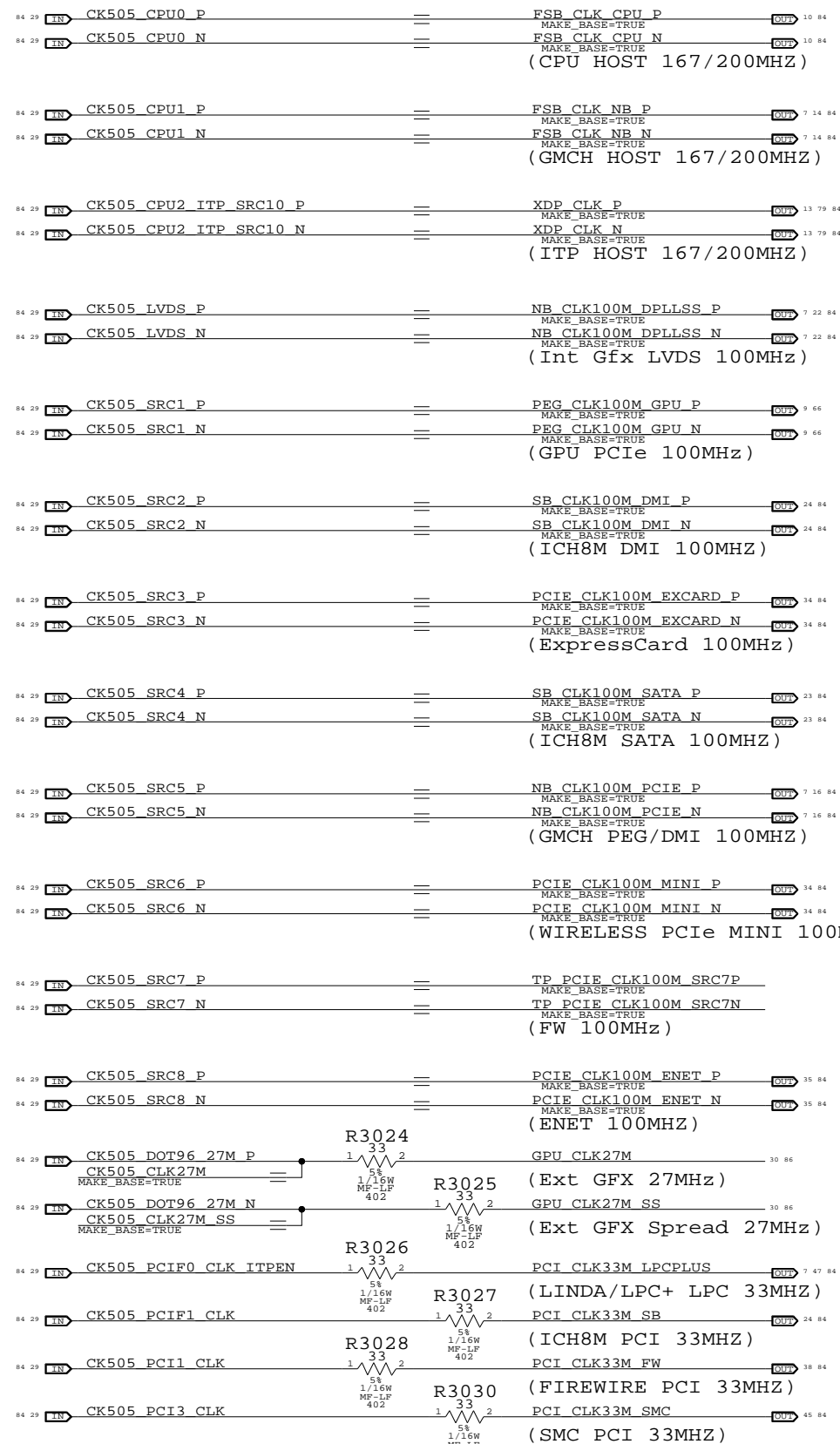


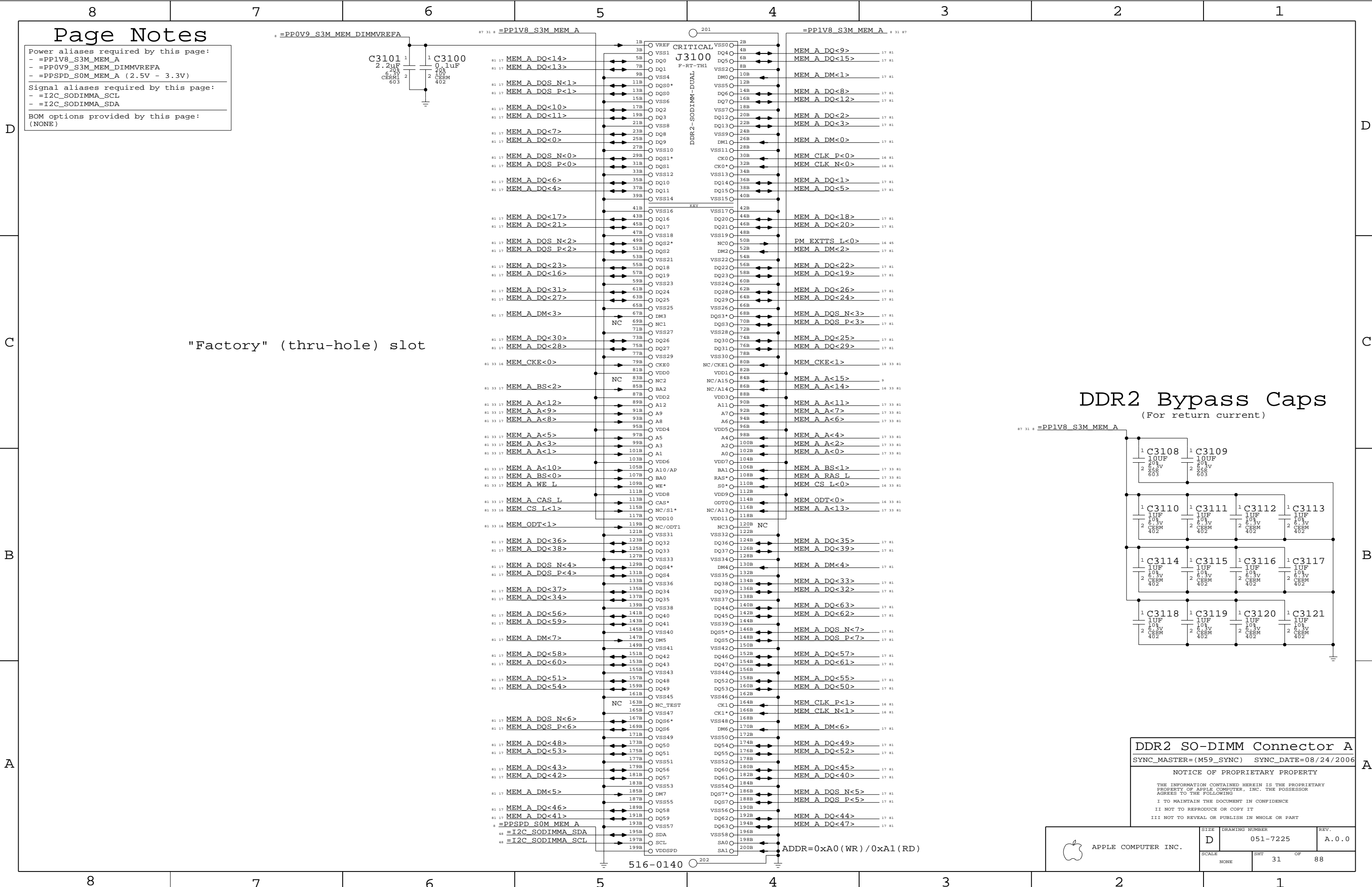
NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

D



B





Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

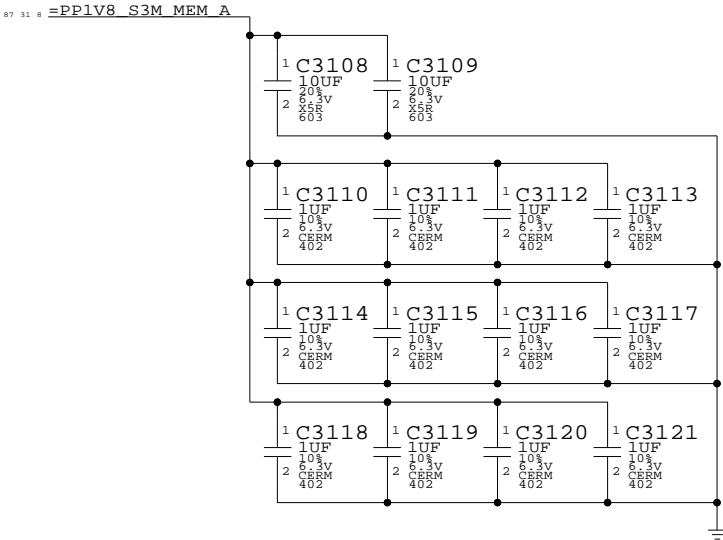
BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

D

051-7225

A.0.0

SCALE

NONE

SHT

31

OF

88

```

Power aliases required by this page:
- =PPIV8_S3M_MEM_B
- =PPOV9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

```

DDR2 Bypass Caps



NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

I NOT TO REPRODUCE OR COPY IT

I NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE
D

NUMBER
051-7225

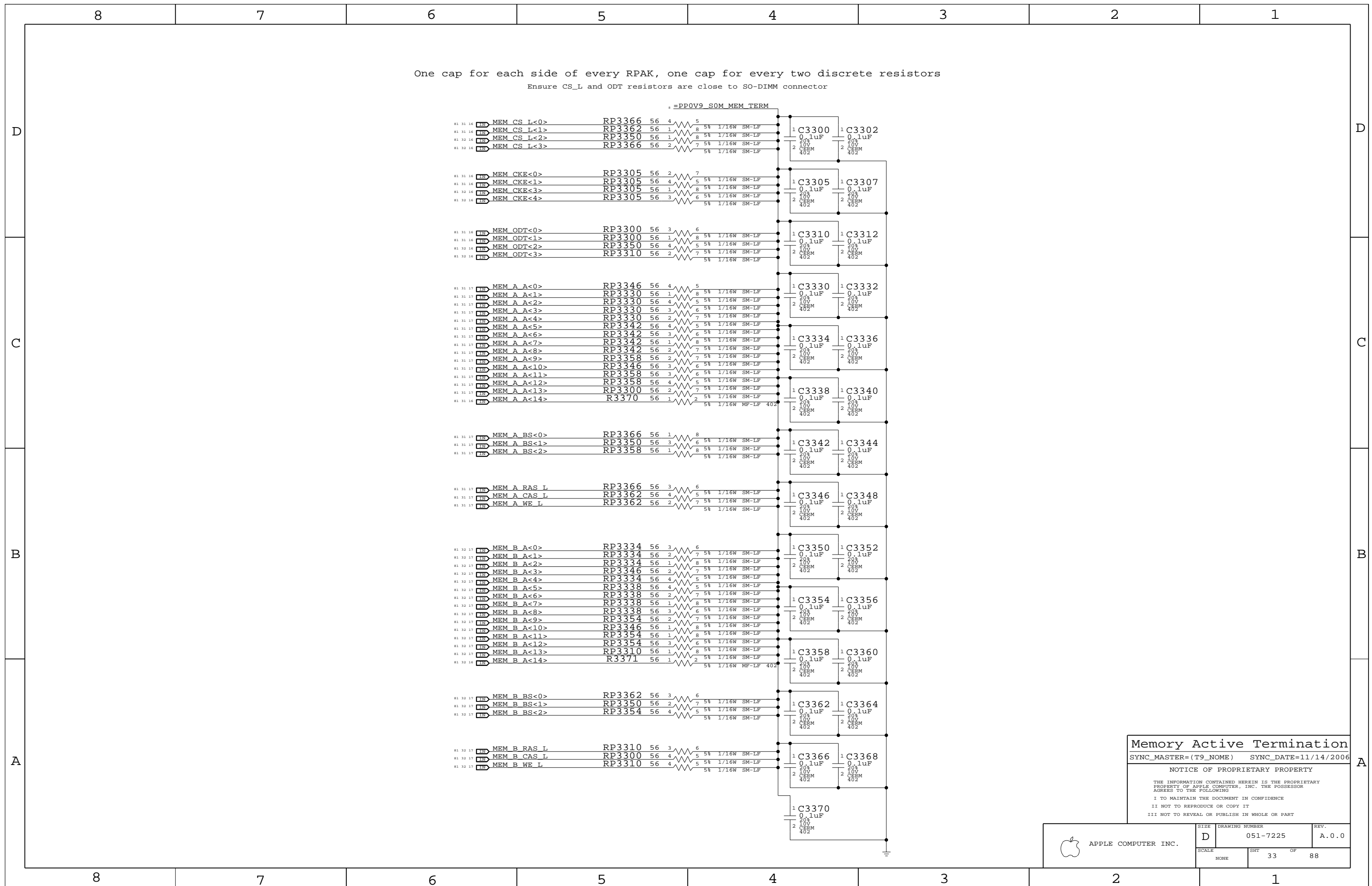
REV.
A.0.0

SCALE

SHT

OF

88



D



D

C

E

B

A

8

APPLE COMPUTER INC.

7

6

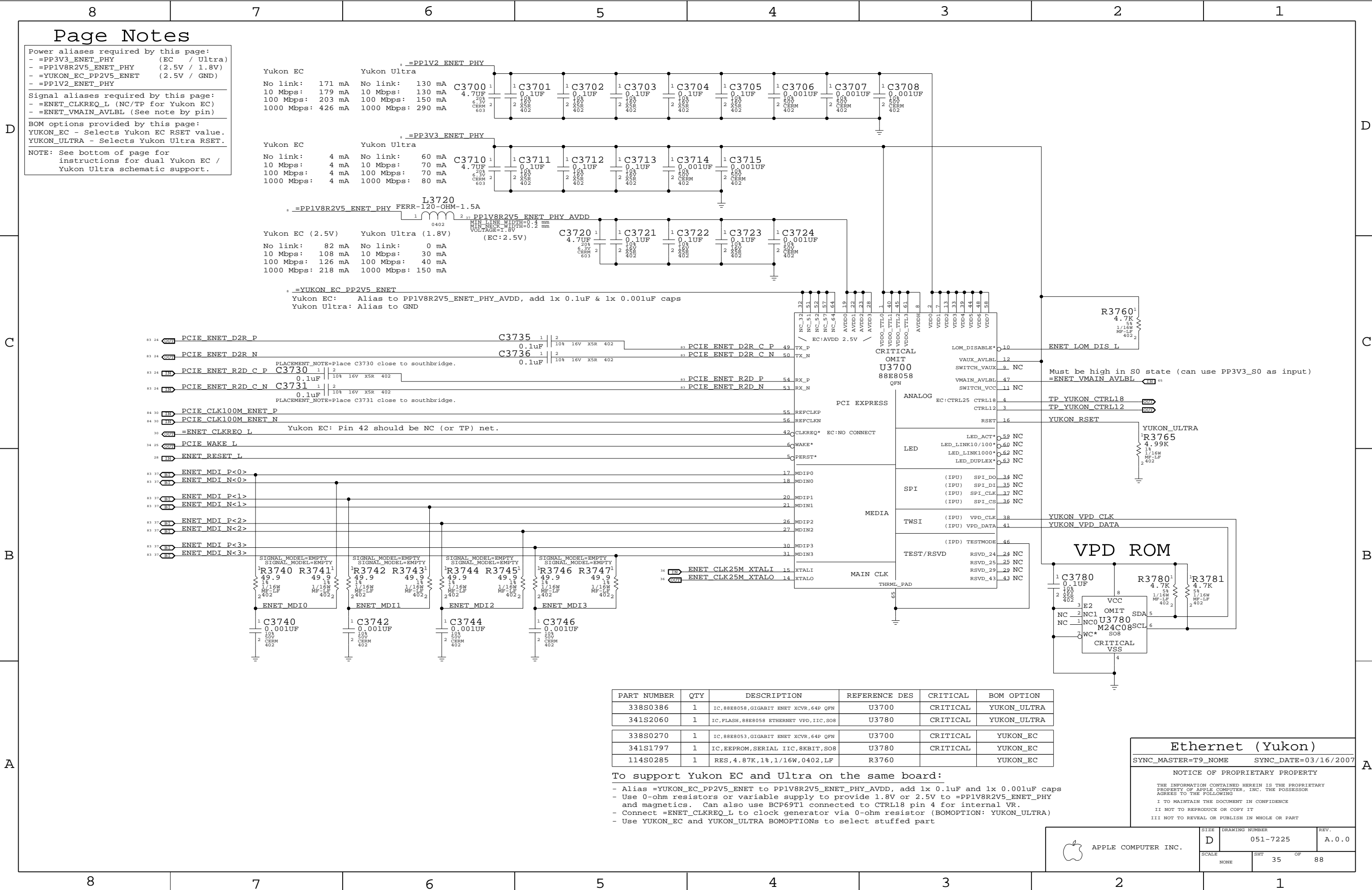
5

4

(v)

2

—



D

C

B

A

D

C

B

A

D

C

B

D



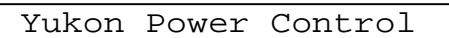
B

A

Yukon Crystal



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC



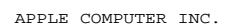
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



8

7

6

5

4

3

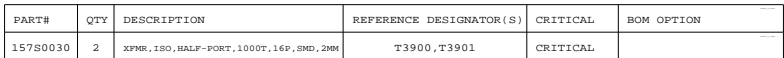
2

1

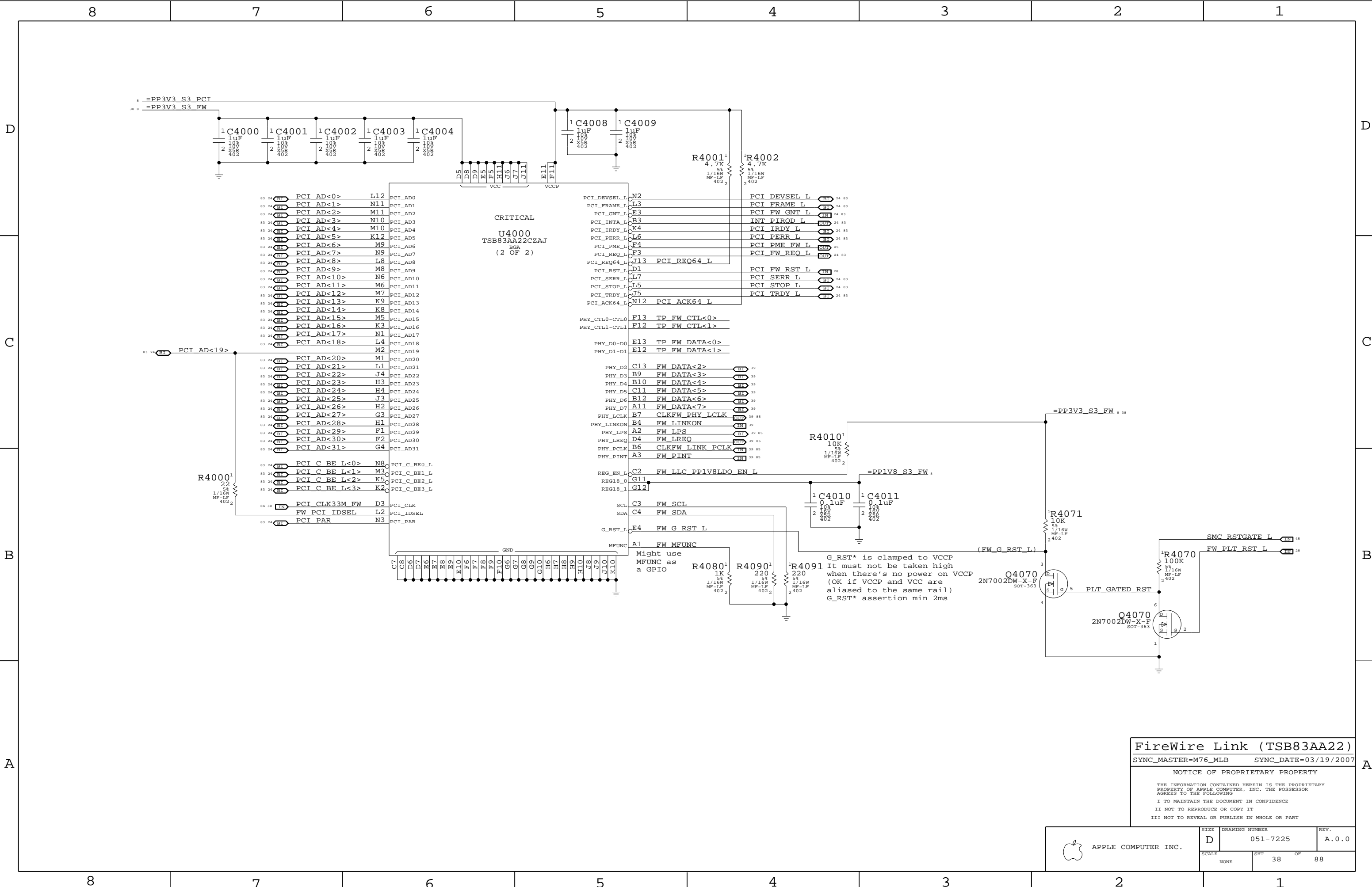
Power aliases required by this page:
=GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
NOTICE OF PROPRIETARY PROPERTY	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING	
I 1 TO MAINTAIN THE DOCUMENT IN CONFIDENCE	
I 2 NOT TO REPRODUCE OR COPY IT	
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

NONE

SHT

38

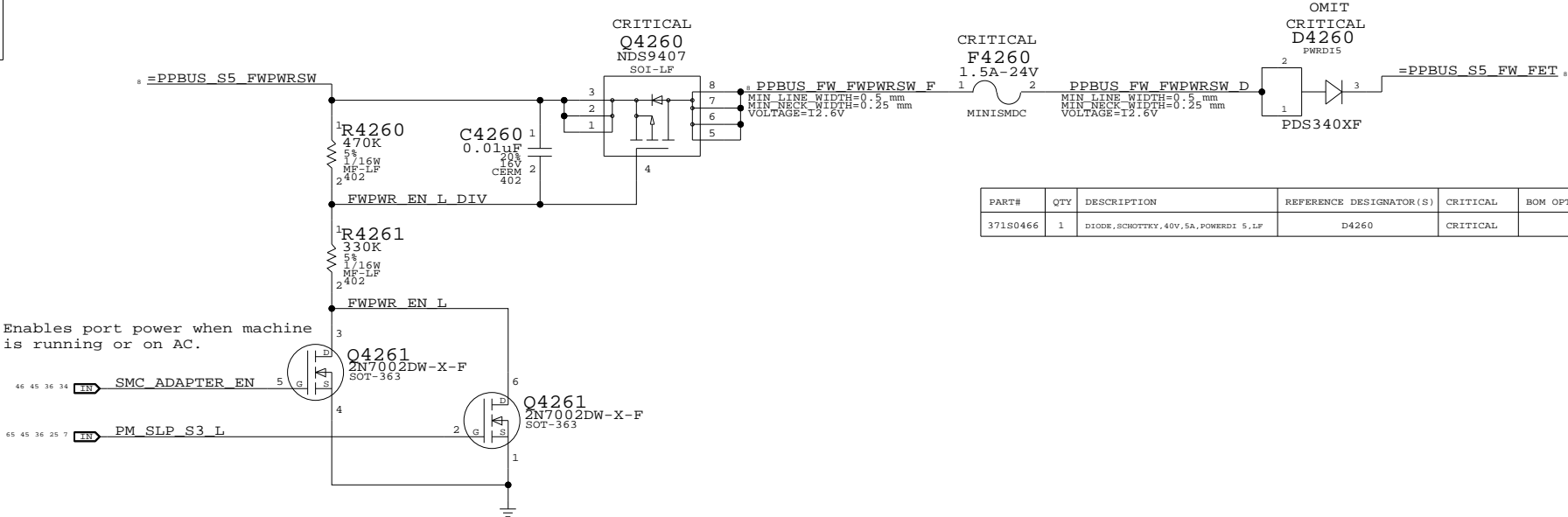
OF

88

Page Notes

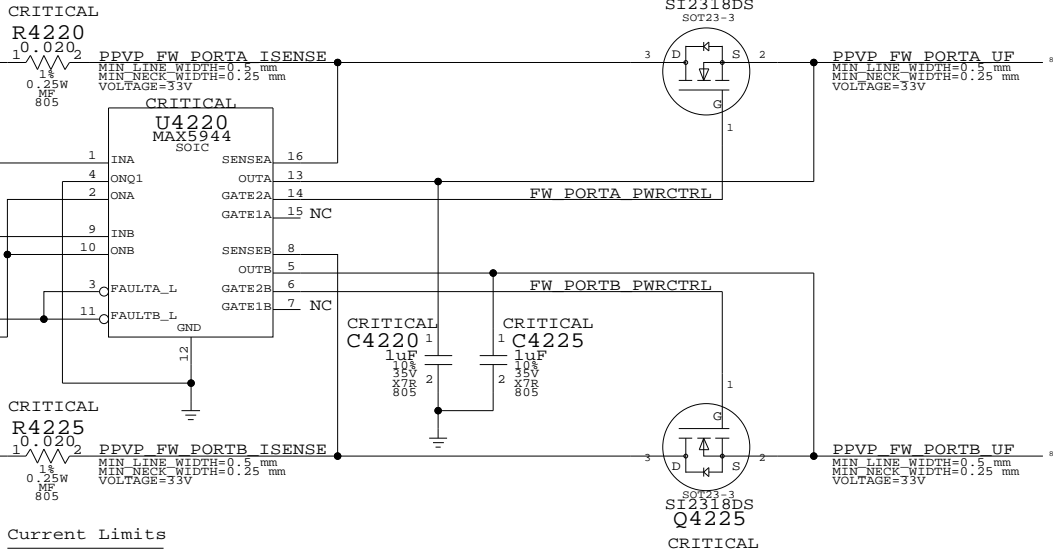
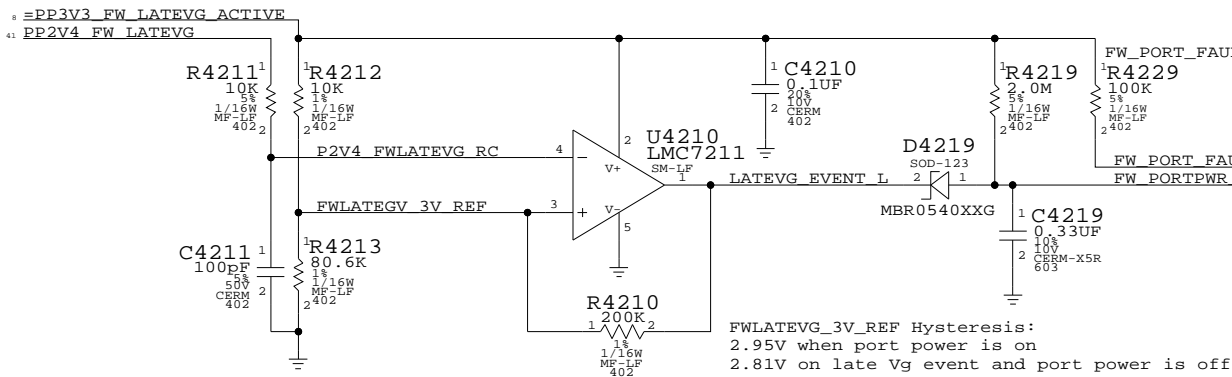
Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	40	88

FireWire PHY Config Straps

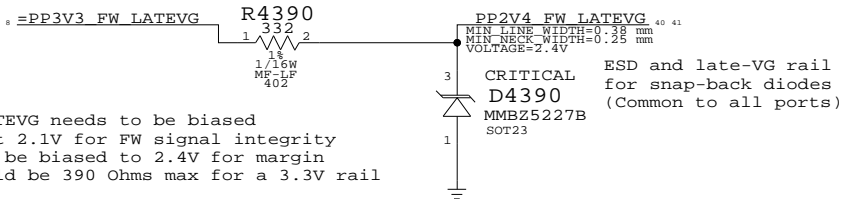
Termination

```

FW 1 TPBIAS
FW 0 TPBIAS
FW 0 TPA P
FW 0 TPA N
FW 0 TPB P
FW 0 TPB N
FW 1 TPA P
FW 1 TPA N
FW 1 TPB P
FW 1 TPB N
FW PORT0 TPB C
FW PORT1 TPB C

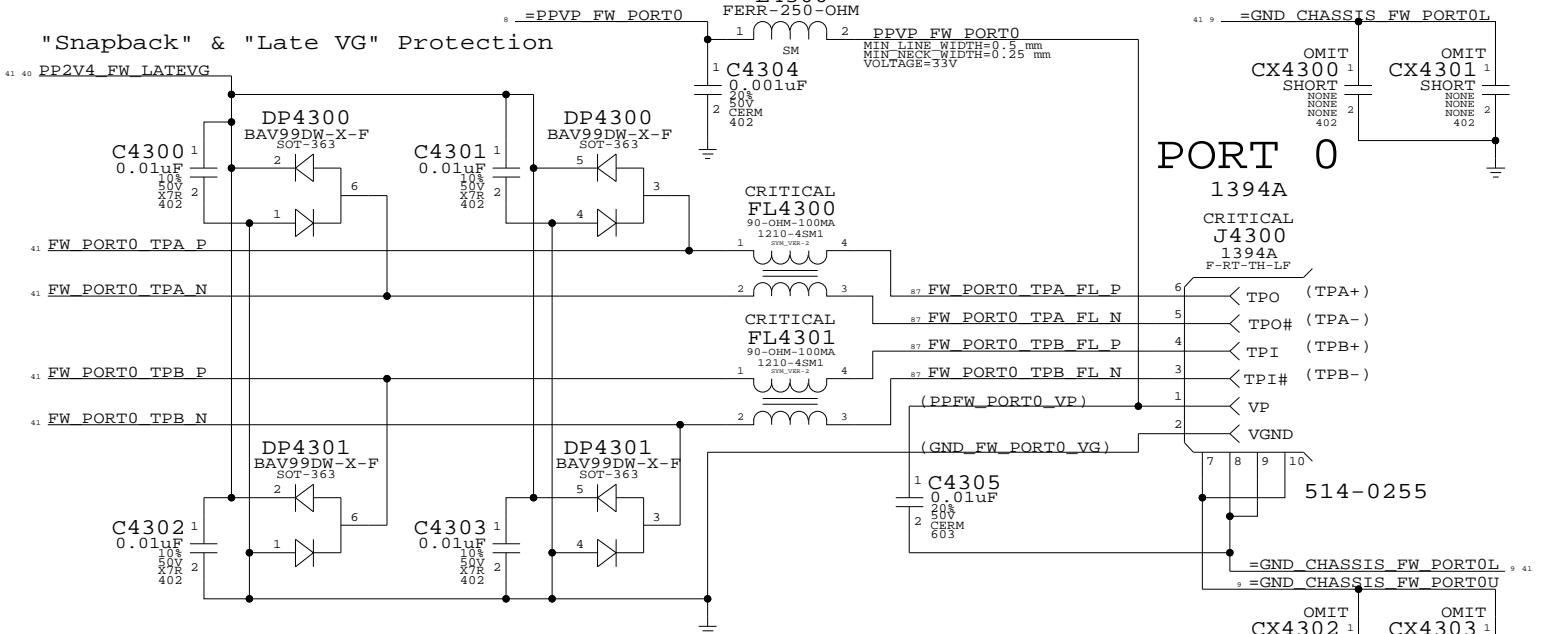
```

Late-VG Protection Power

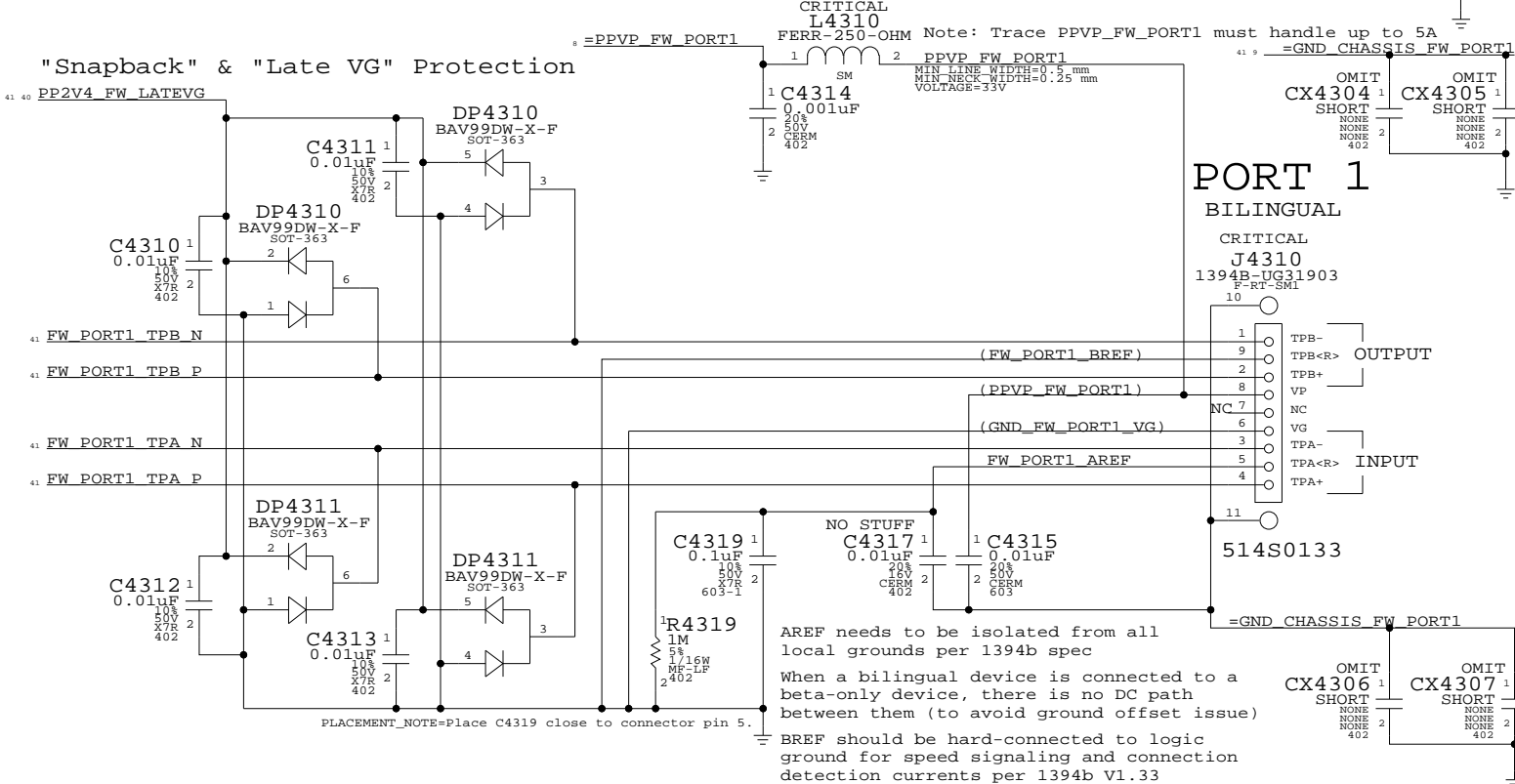


PP2V4_FWLATEVG needs to be biased
to at least 2.1V for FW signal integrity
and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



FireWire Ports

SOURCE=SYNCHRONIZATION
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZ

DRAWING NUMBER

REV.

SCALE

SHT

OF

SCALE

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

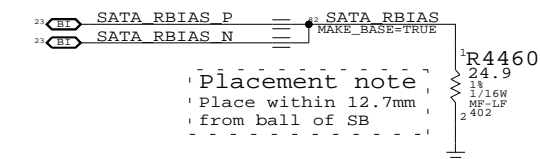


C

B

A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
-----------------------	---------------------

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
IF NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

[illegible]

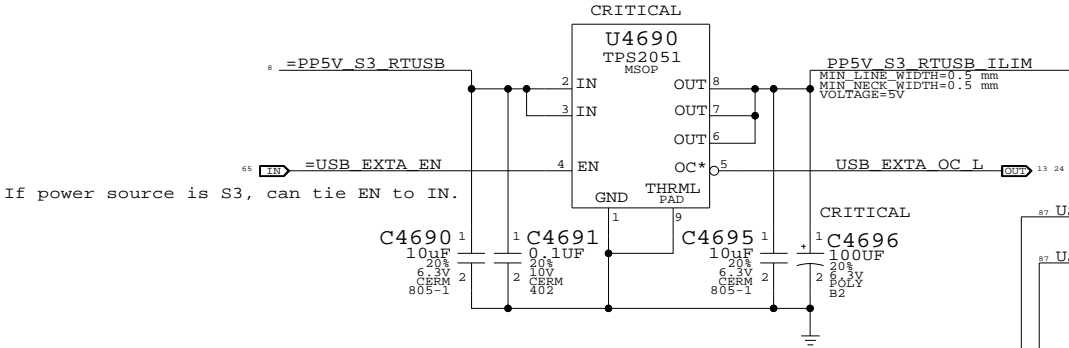
COMPUTER, INC.	D	051-7225	A.0.0
----------------	---	----------	-------

	NONE	42	88
--	------	----	----

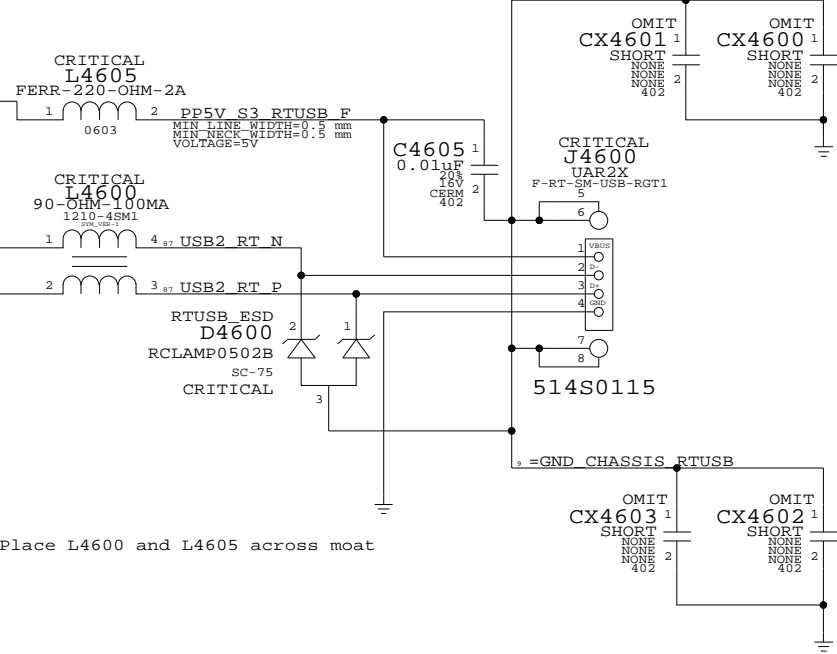
	1
--	---

I

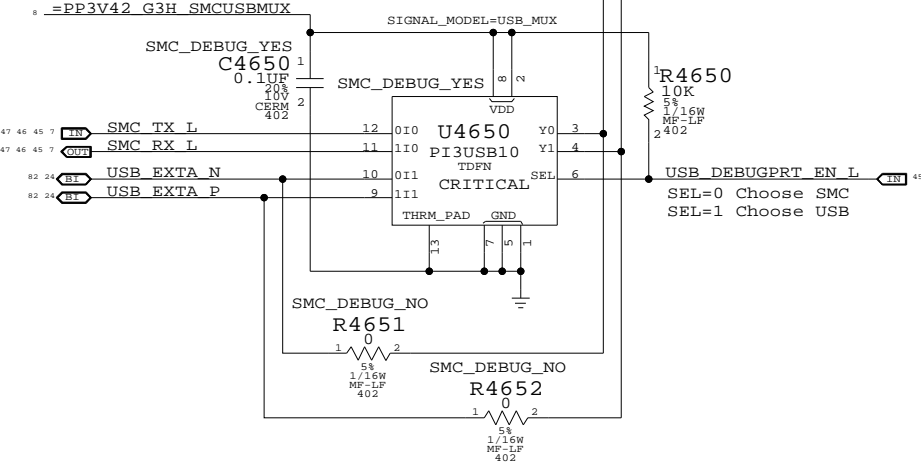
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

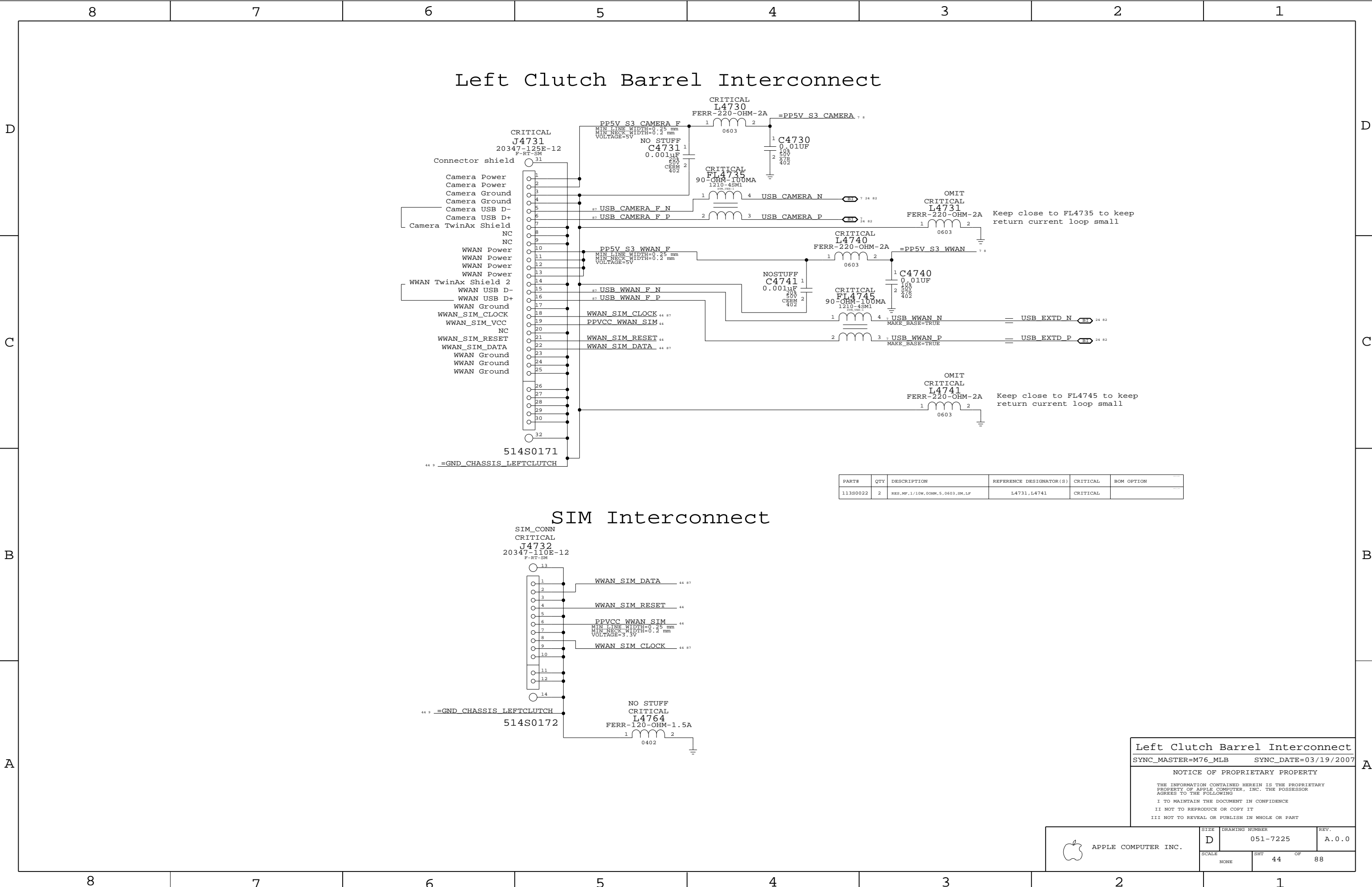
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	43	88



Left Clutch Barrel Interconnect
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

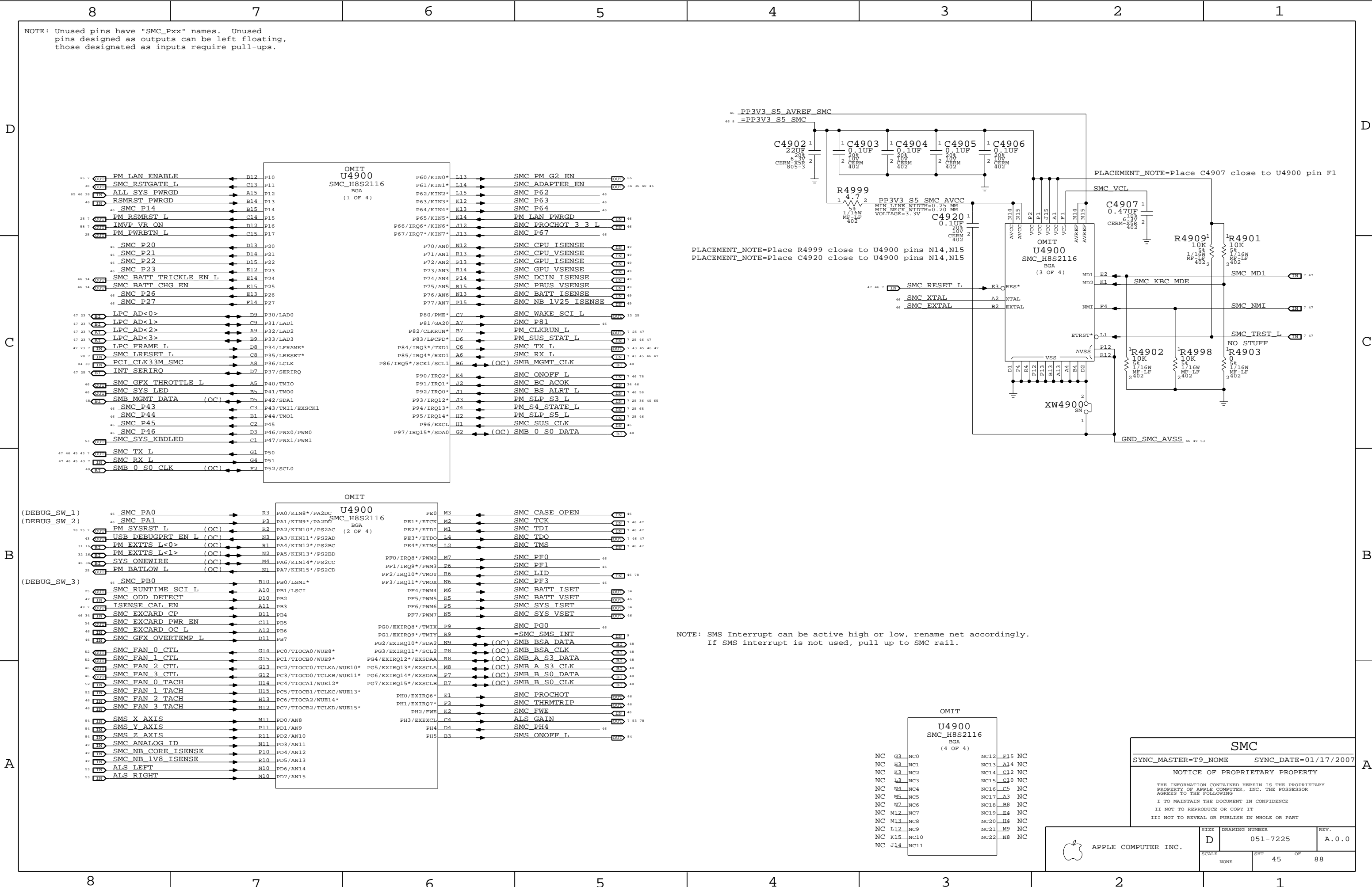
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

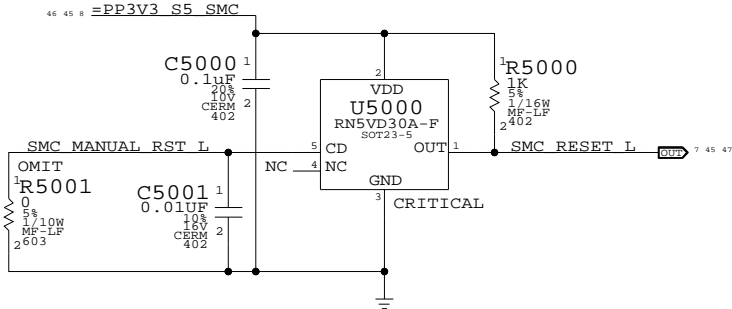
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

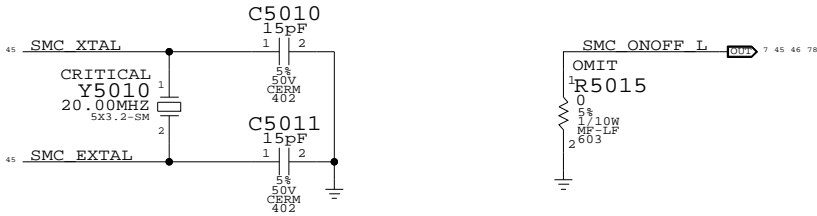
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 44	OF 88



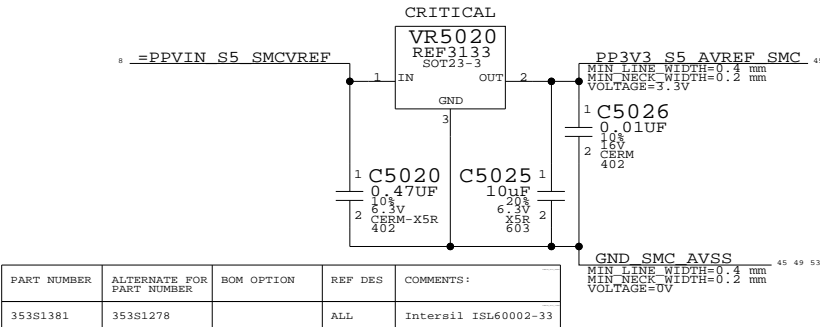
SMC Reset "Button" / Brownout Detect



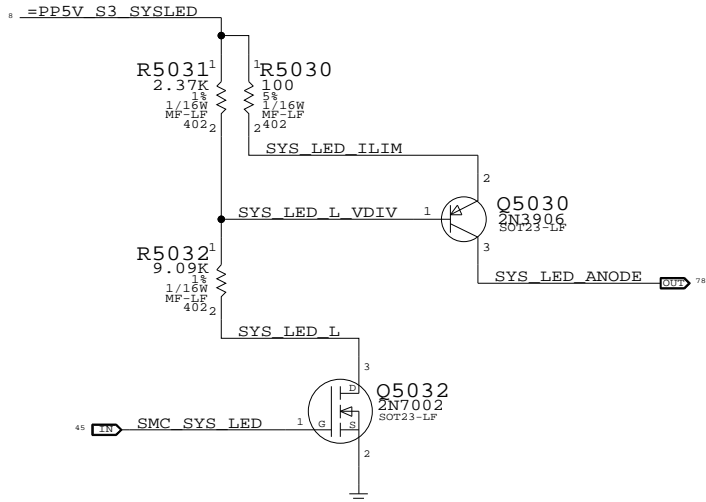
SMC Crystal Circuit Debug Power "Button"



SMC AVREF Supply



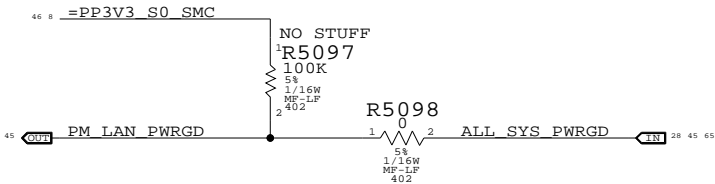
System (Sleep) LED Circuit



SMC FAN 2 CTL	=	TP_SMC_FAN_2_CTL
SMC FAN 2 TACH	=	TP_SMC_FAN_2_TACH
SMC FAN 3 CTL	=	TP_SMC_FAN_3_CTL
SMC FAN 3 TACH	=	TP_SMC_FAN_3_TACH
SMC GFX OVERTEMP_L	=	TP_SMC_GFX_OVERTEMP_L
SMC GFX THROTTLE_L	=	TP_SMC_GFX_THROTTLE_L
SMC BATT VSET	=	TP_SMC_BATT_VSET
SMC SYS VSET	=	TP_SMC_SYS_VSET
SMC P14	=	TP_SMC_P14
SMC P20	=	TP_SMC_P20
SMC P21	=	TP_SMC_P21
SMC P22	=	TP_SMC_P22
SMC P23	=	TP_SMC_P23
SMC P26	=	TP_SMC_P26
SMC P27	=	TP_SMC_P27
SMC P43	=	TP_SMC_P43
SMC P44	=	TP_SMC_P44
SMC P46	=	TP_SMC_P46
SMC P62	=	TP_SMC_P62
SMC P63	=	TP_SMC_P63
SMC P64	=	TP_SMC_P64
SMC P81	=	TP_SMC_P81
SMC PF0	=	TP_SMC_PF0
SMC PF1	=	TP_SMC_PF1

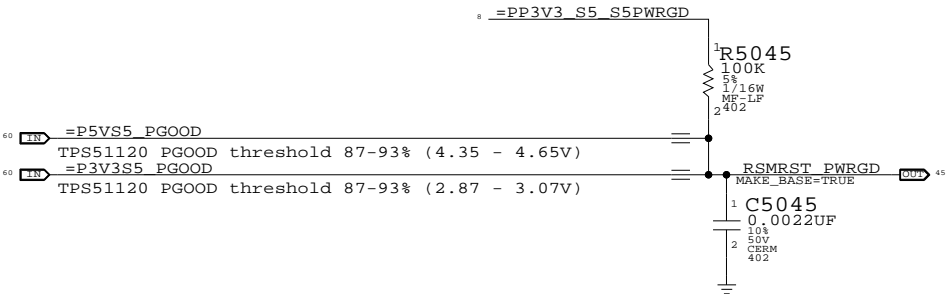
SMC EXCARD_OC_L	=	EXCARD_OC_L
SMC_SUS_CLK	=	SUS_CLK_SB
SMC_P45	=	SMC_ENRGYSTR_LDO_EN

LAN PWRGD Circuit

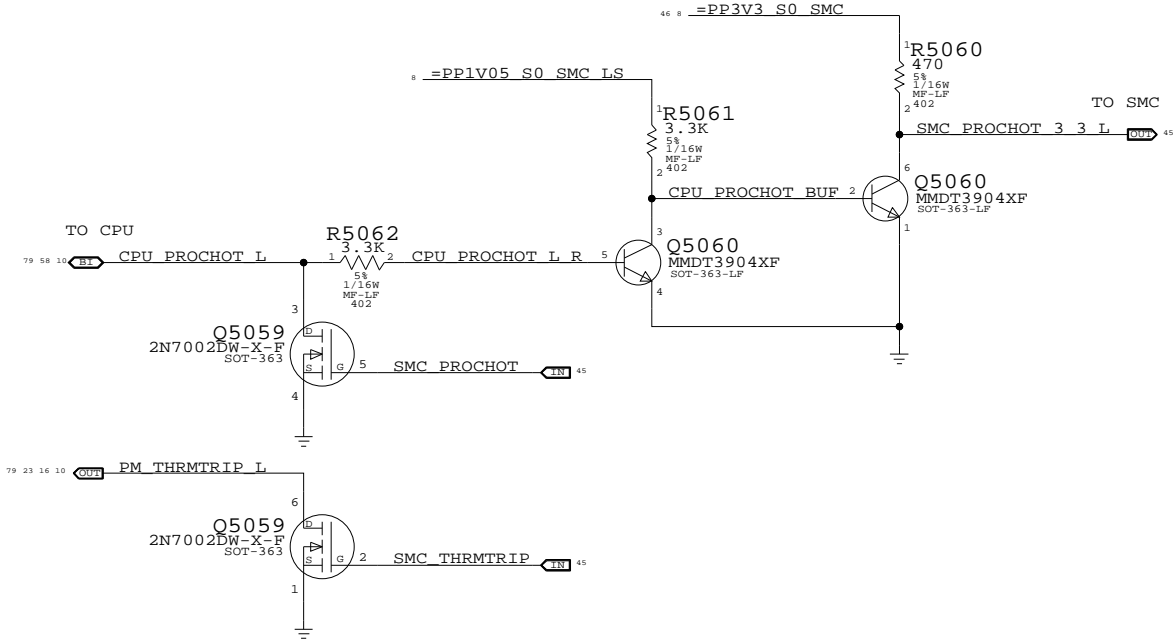


S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting



SMC_PA0	R5091	100K	5%	1/16W MF-LF 402
SMC_PA1	R5092	100K	5%	1/16W MF-LF 402
SMC_PB0	R5093	100K	5%	1/16W MF-LF 402
SMC_ONOFF_L	R5070	10K	5%	1/16W MF-LF 402
SMC_LID	R5071	100K	5%	1/16W MF-LF 402
SMC_FWE	R5072	10K	5%	1/16W MF-LF 402
SMC_TX_L	R5073	10K	5%	1/16W MF-LF 402
SMC_RX_L	R5074	100K	5%	1/16W MF-LF 402
SYS_ONEWIRE	R5075	2.0K	5%	1/16W MF-LF 402
SMC_BS_ALRT_L	R5076	100K	5%	1/16W MF-LF 402
SMC_TMS	R5077	10K	5%	1/16W MF-LF 402
SMC_TDO	R5078	10K	5%	1/16W MF-LF 402
SMC_TDI	R5079	10K	5%	1/16W MF-LF 402
SMC_TCK	R5080	10K	5%	1/16W MF-LF 402
SMC_P67	R5094	10K	5%	1/16W MF-LF 402
SMC_PF3	R5081	10K	5%	1/16W MF-LF 402
SMC_PG0	R5096	10K	5%	1/16W MF-LF 402
SMC_PH4	R5082	10K	5%	1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L	R5083	10K	5%	1/16W MF-LF 402
SMC_BATT_CHG_EN	R5084	10K	5%	1/16W MF-LF 402
SMC_ADAPTER_EN	R5085	10K	5%	1/16W MF-LF 402
SMC_CASE_OPEN	R5086	10K	5%	1/16W MF-LF 402
SMC_BC_ACOK	R5087	470K	5%	1/16W MF-LF 402
SMC_EXCARD_CP	R5088	10K	5%	1/16W MF-LF 402
PM_SUS_STAT_L	R5089	100K	5%	1/16W MF-LF 402
PM_SLP_S5_L	R5090	100K	5%	1/16W MF-LF 402

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D

051-7225

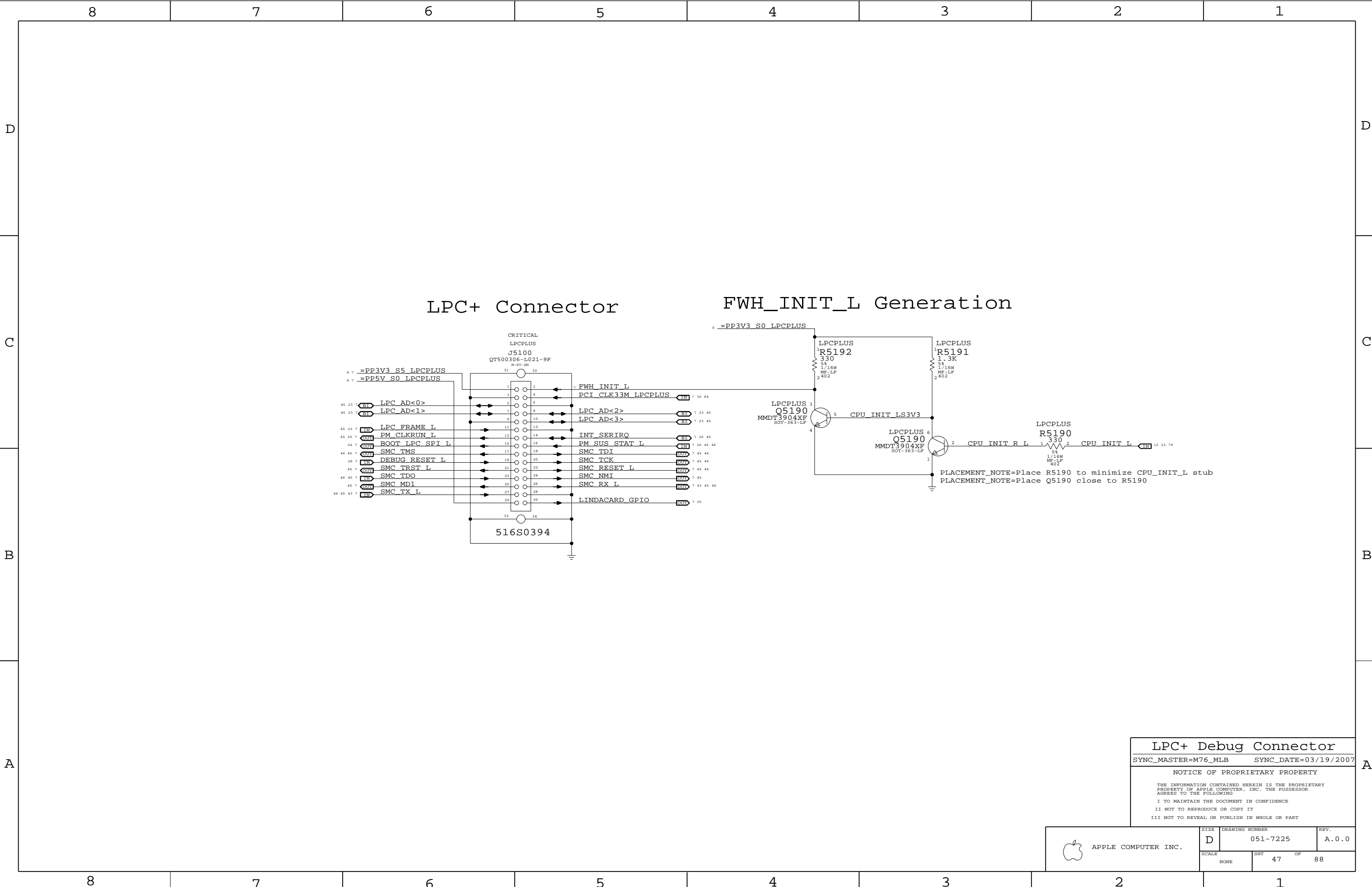
A.0.0

SCALE SHEET OF

NONE

46

88



LPC+ Debug Connector

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007


NOTICE OF PROPRIETARY PROPERTY

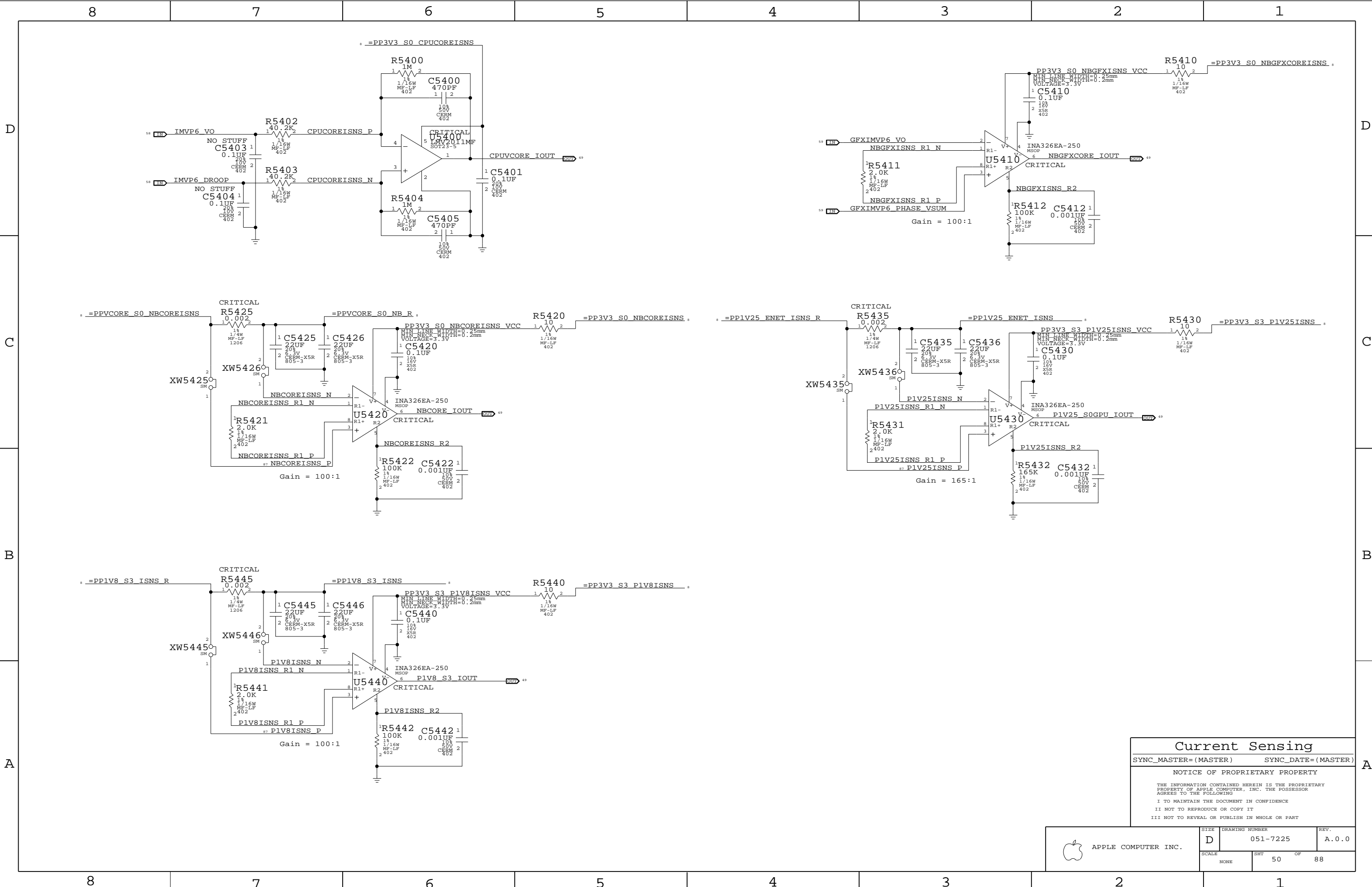
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 47	OF 88



Current Sensing

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

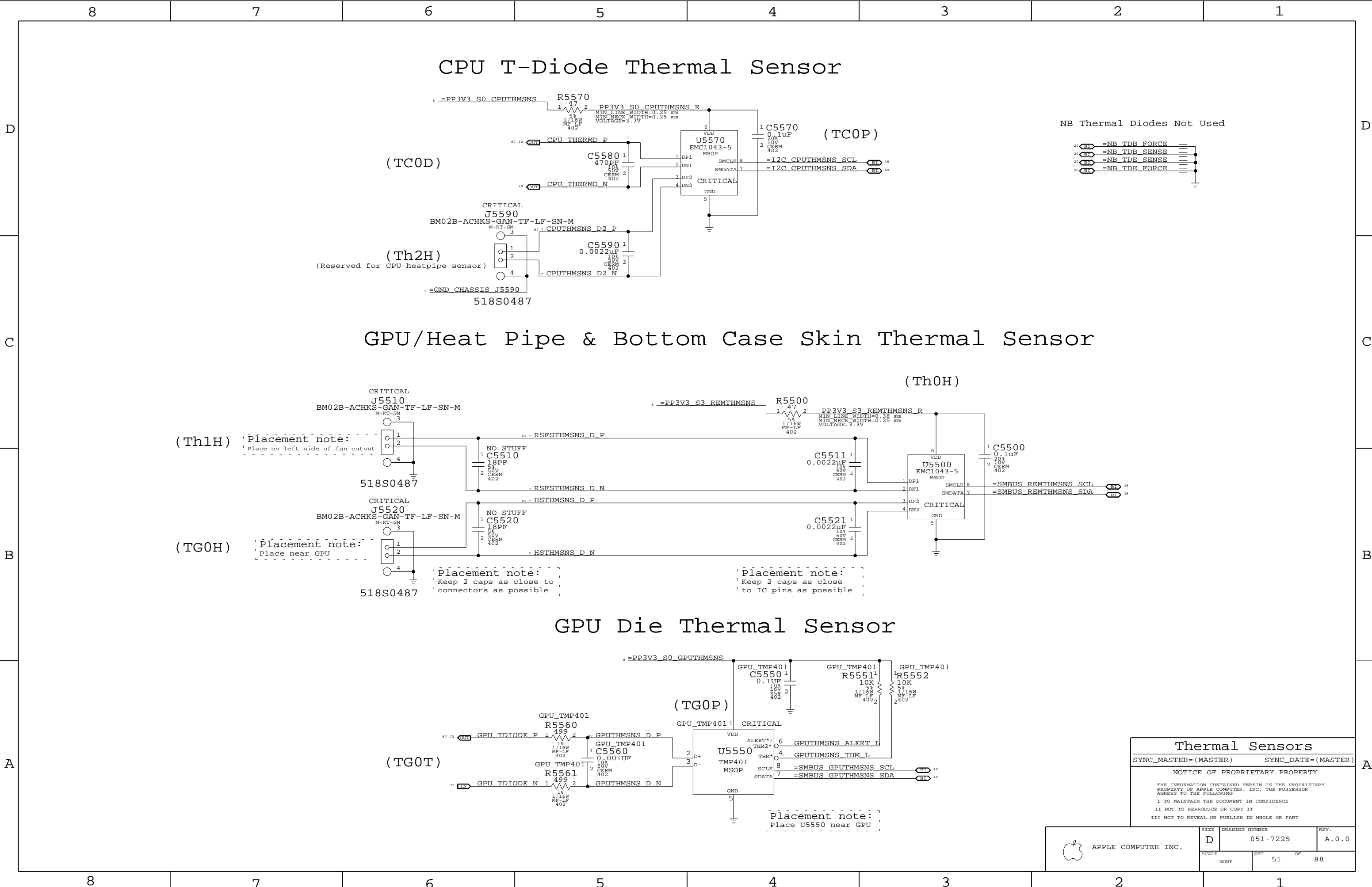
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

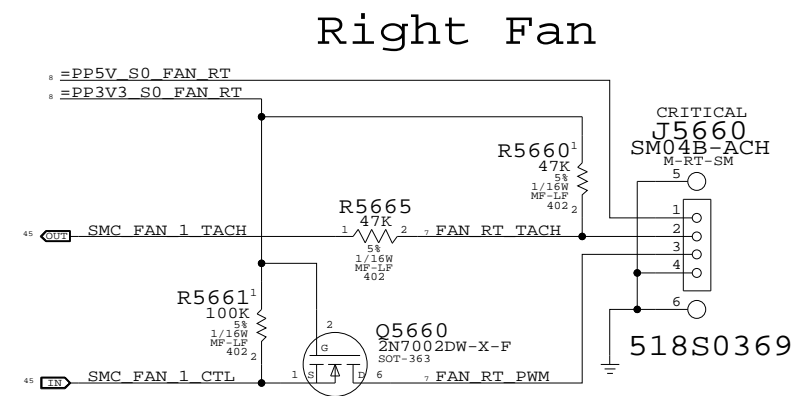
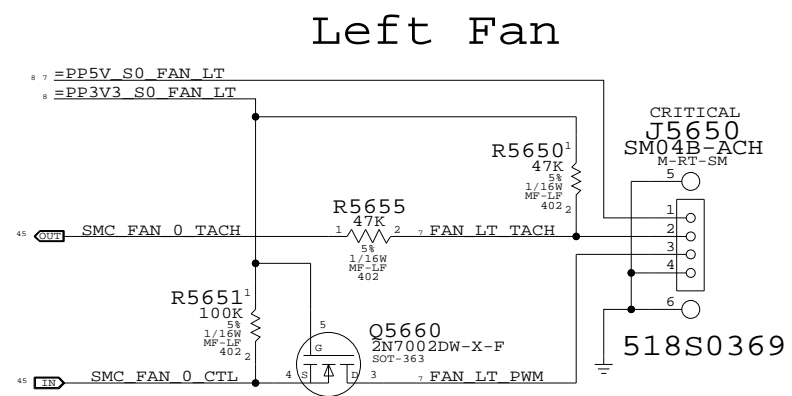
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		50	88





Fan Connectors

SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
---------------------	----------------------

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE
D

D

SIZE	DRAWING NUMBER
D	051-7225

REV.

A.0.0

SCALE	
	NON

NON

SHT

511

OF

54

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

7 A

8

7

6

5

4

3

2

1

D

C

B

A

D

C

B

A

8

7

6

5

4

3

2

1

8

7

6

5

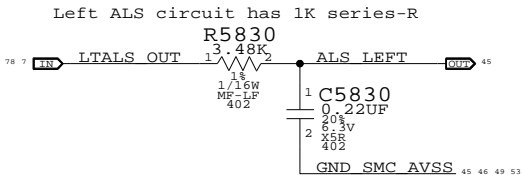
4

3

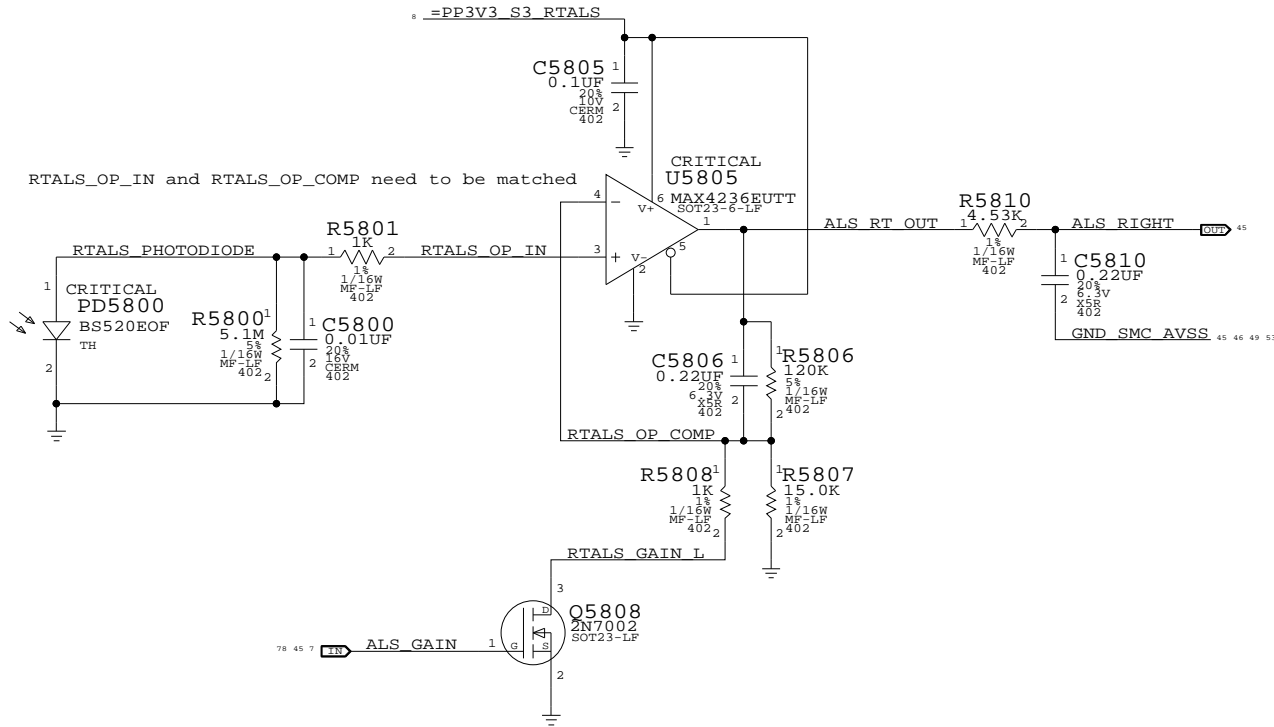
2

1

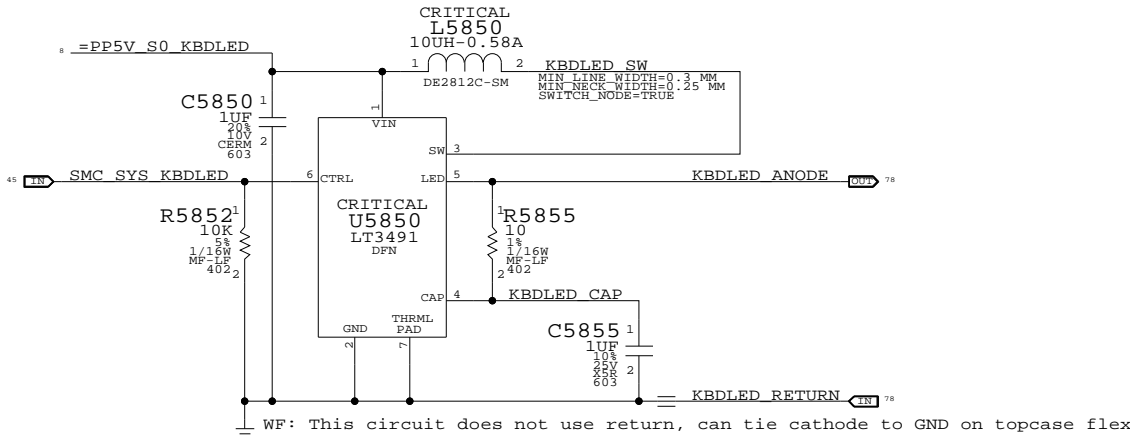
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

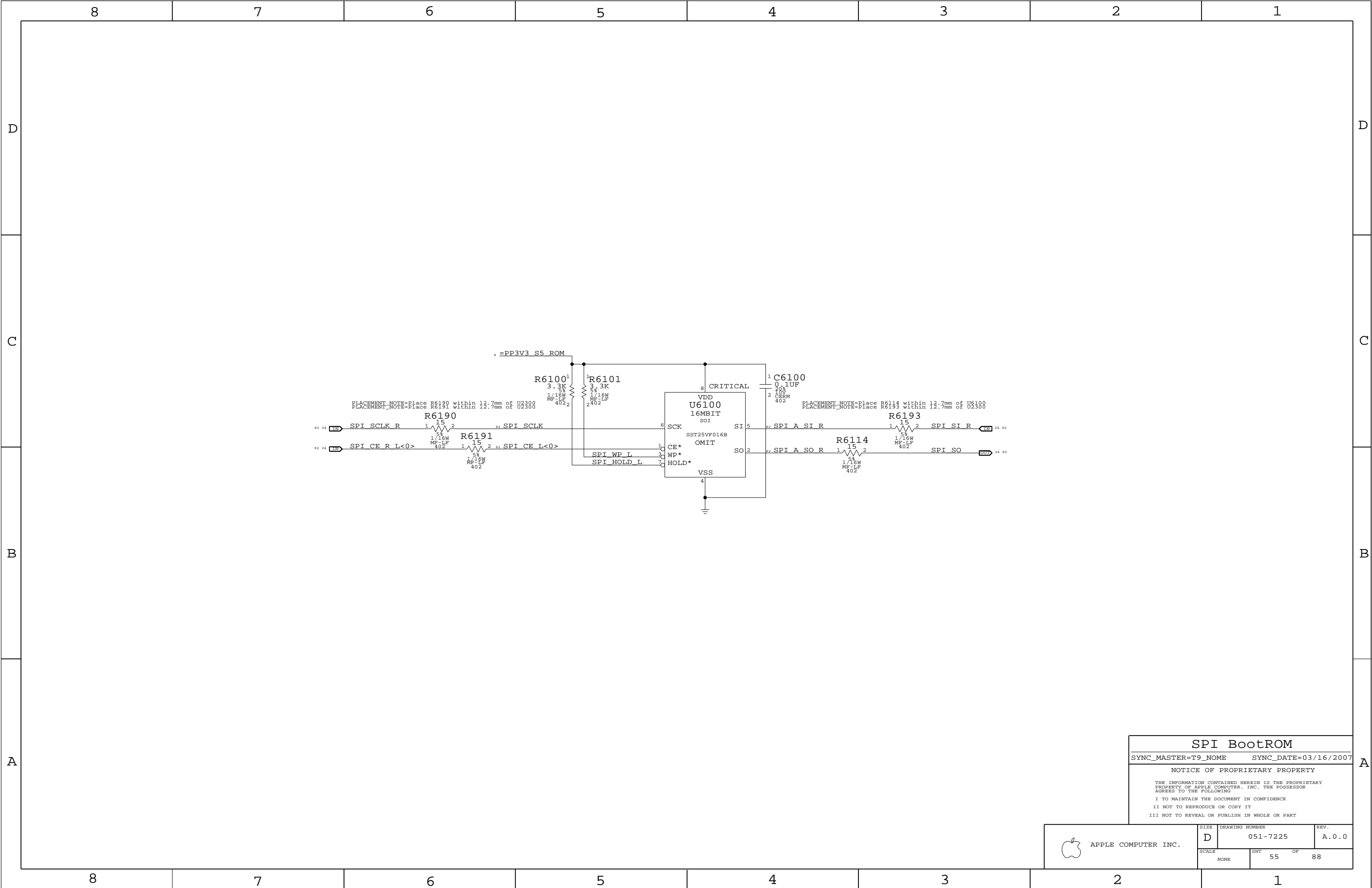
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	53	88



SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

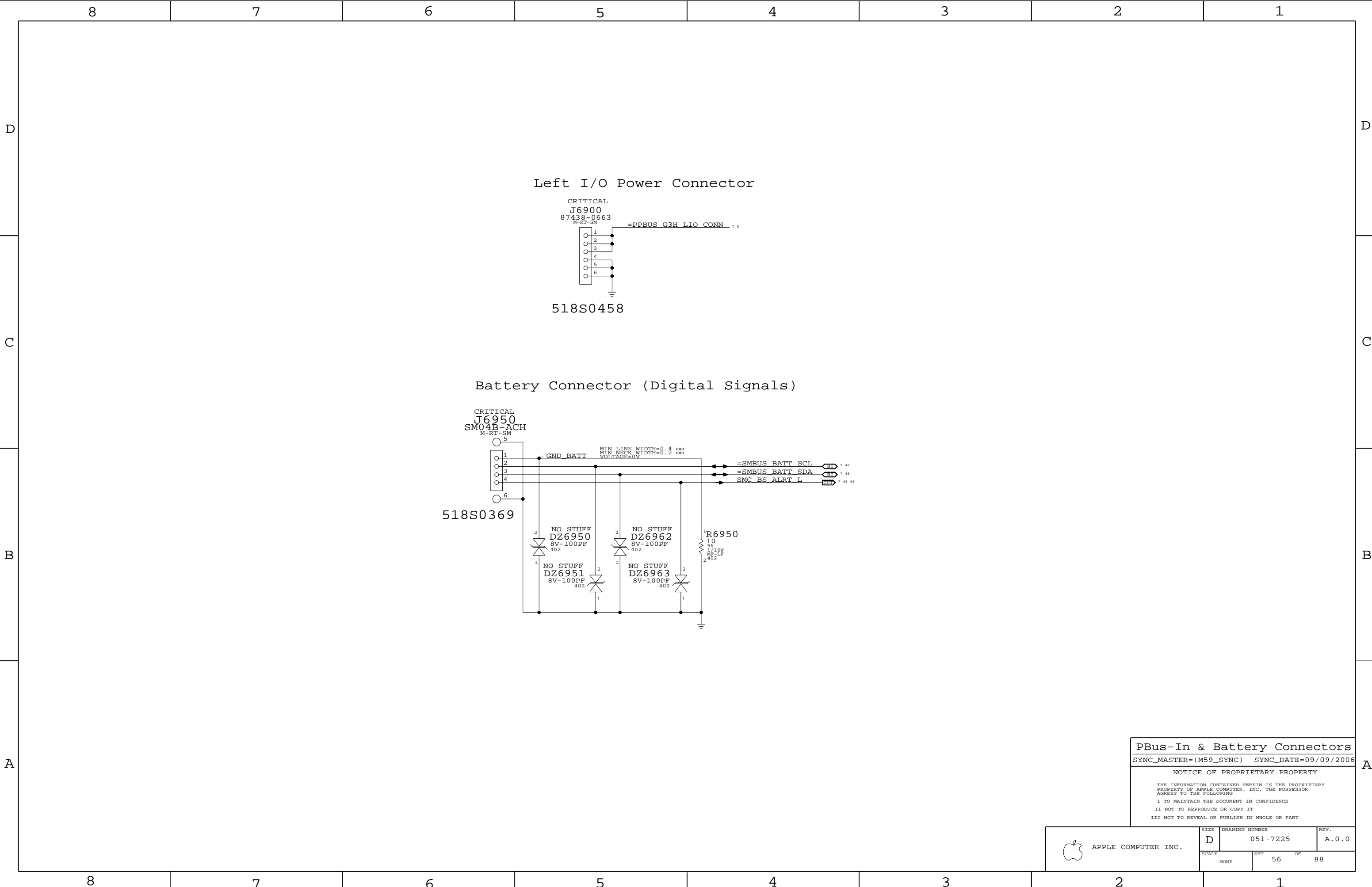
NONE

SHT

55

OF

88



PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

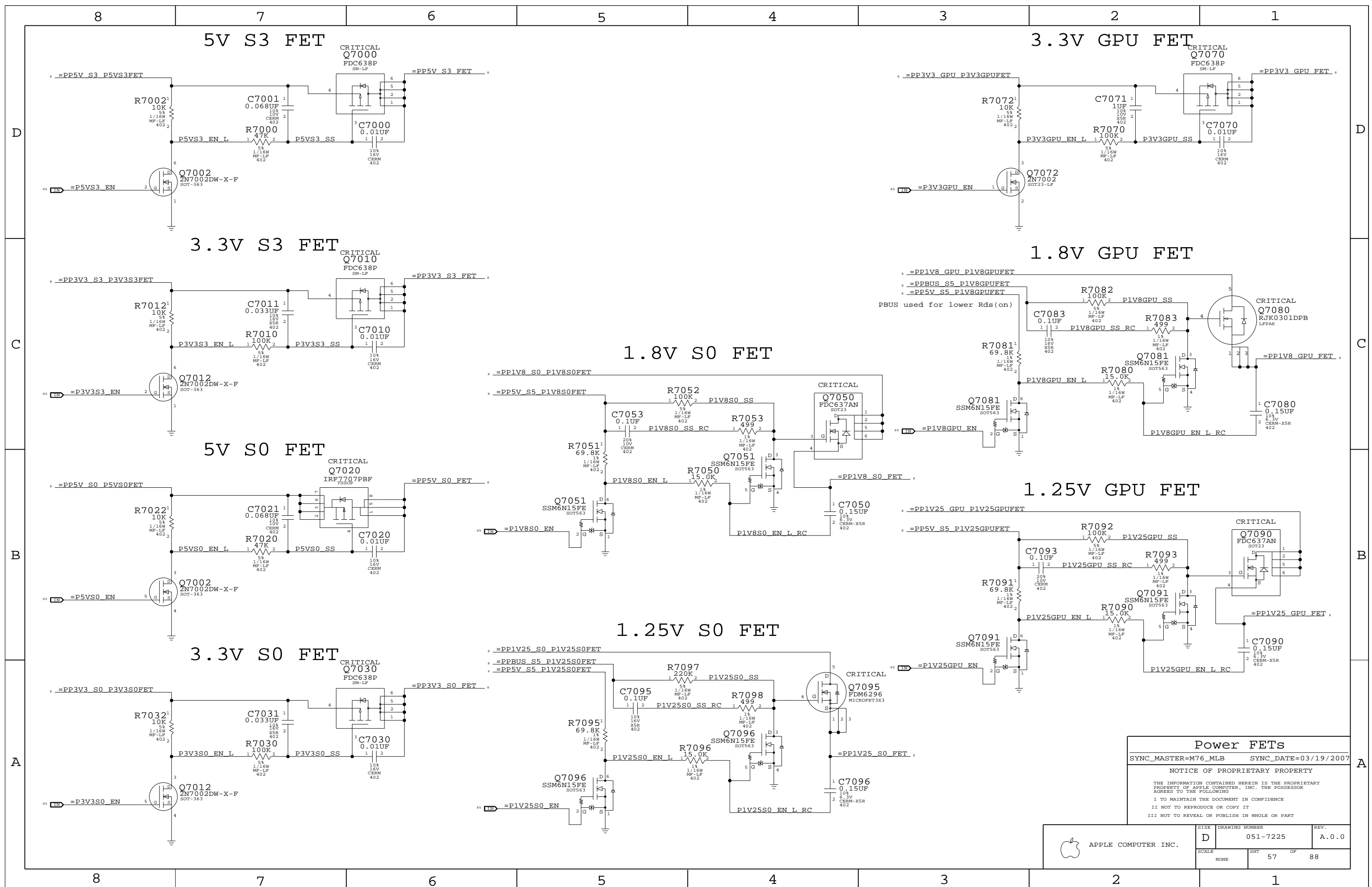
NONE

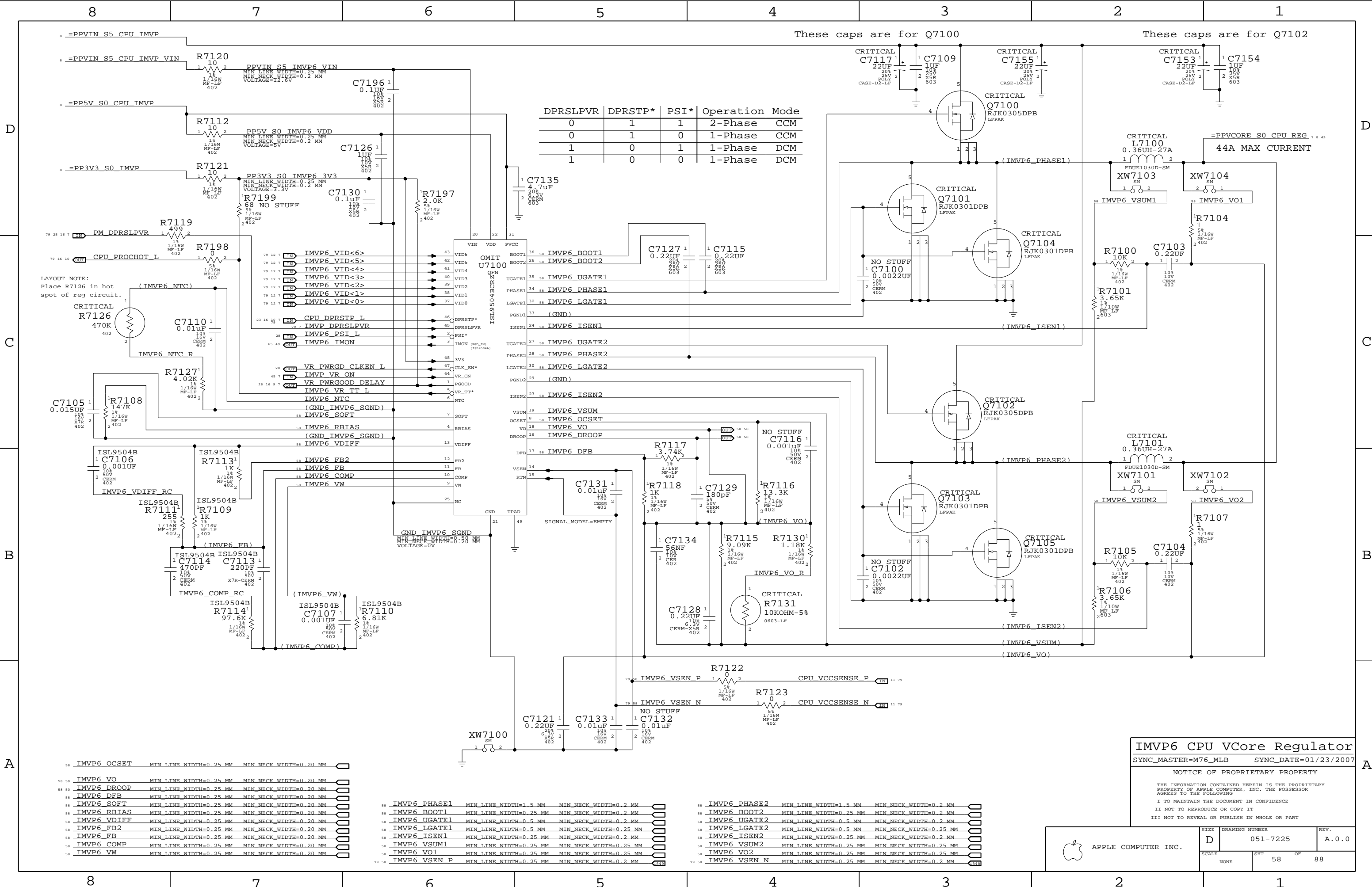
SHT

56

OF

88





DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

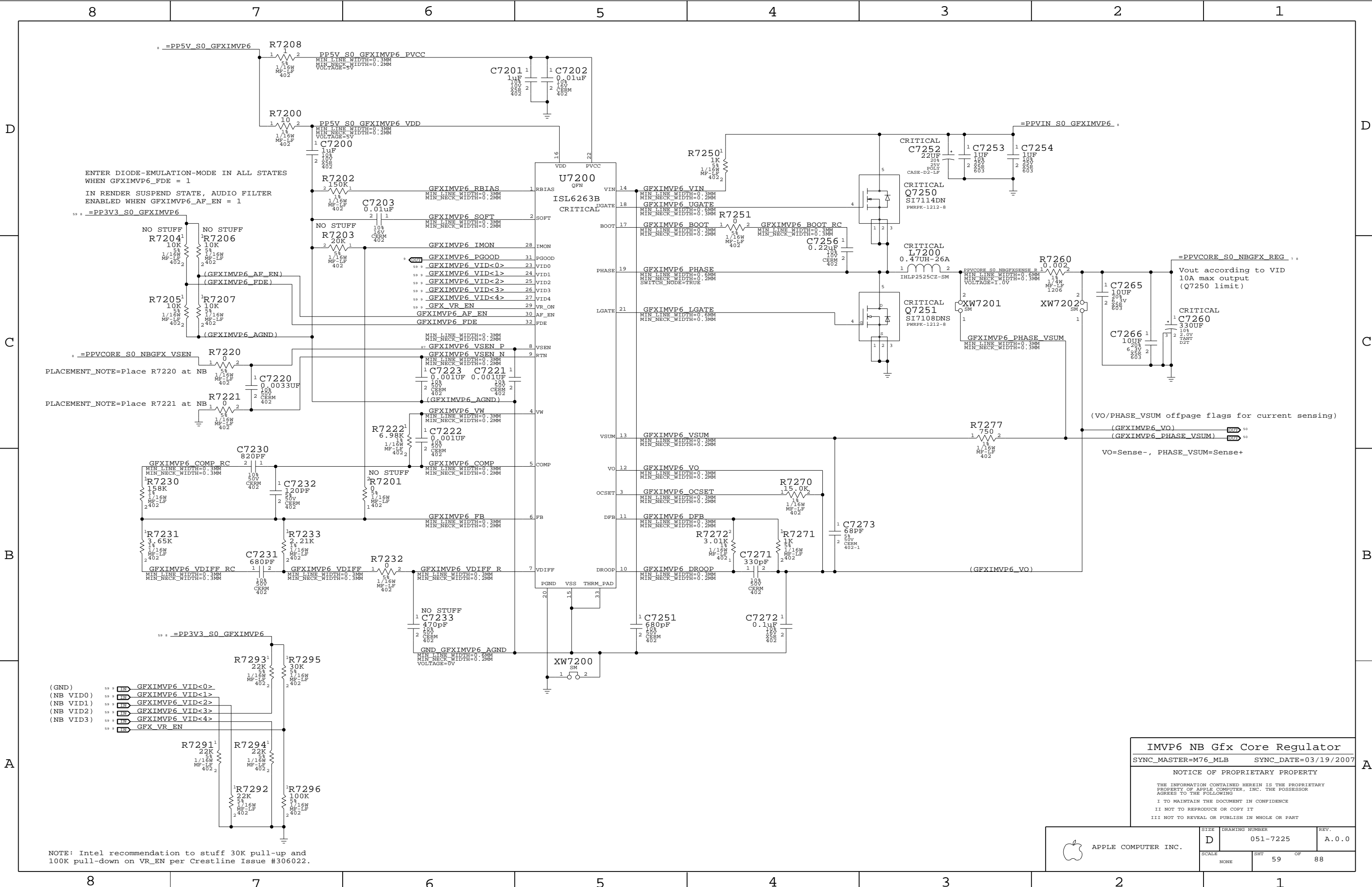
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	58	88



NOTE: Intel recommendation to stuff 30K pull-up and 100K pull-down on VR_EN per Crestline Issue #306022.

IMVP6 NB Gfx Core Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

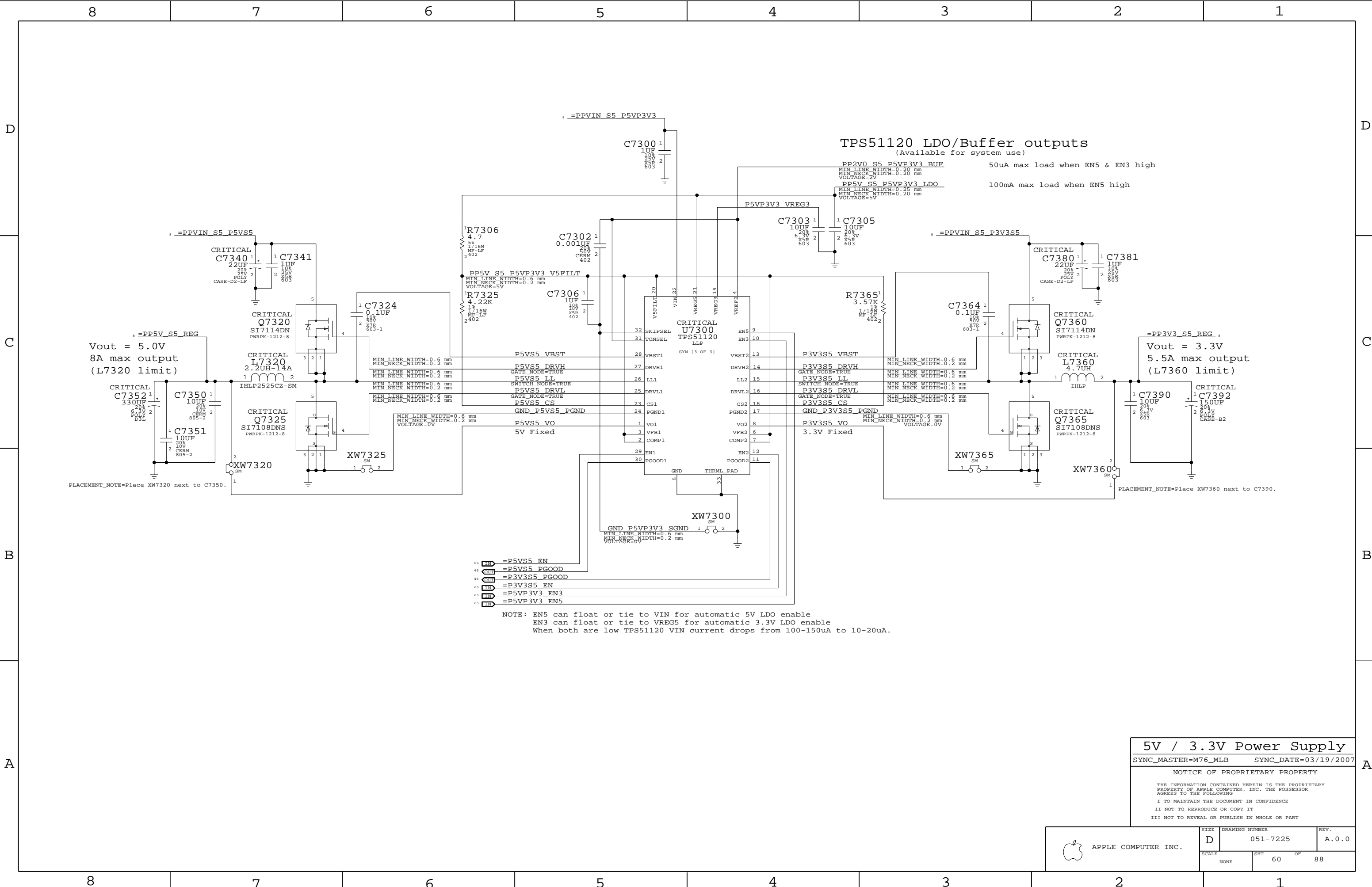
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE	SHT		
	NONE	59	OF 88



NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

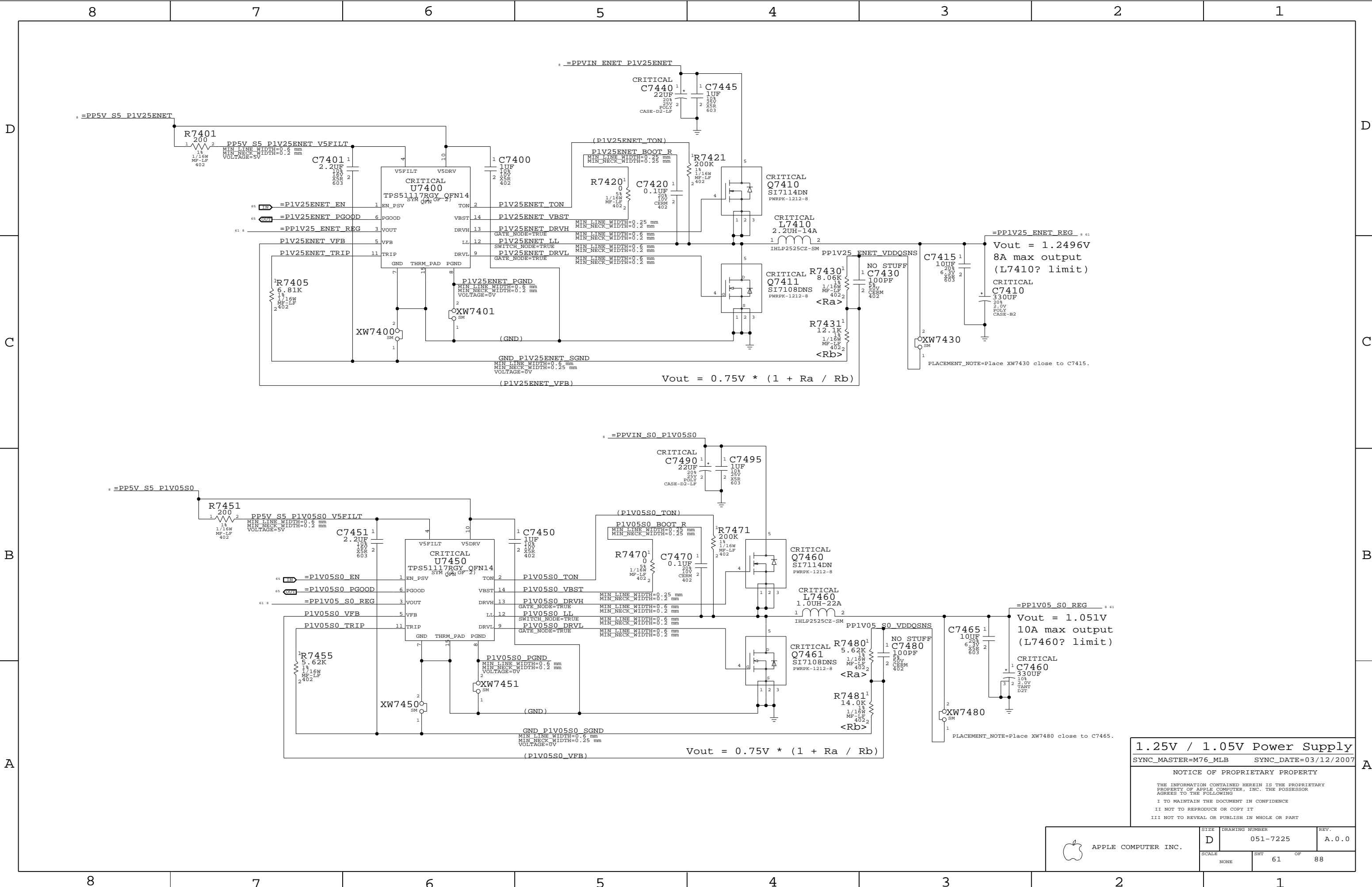
NONE

SHT

60

OF

88



1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

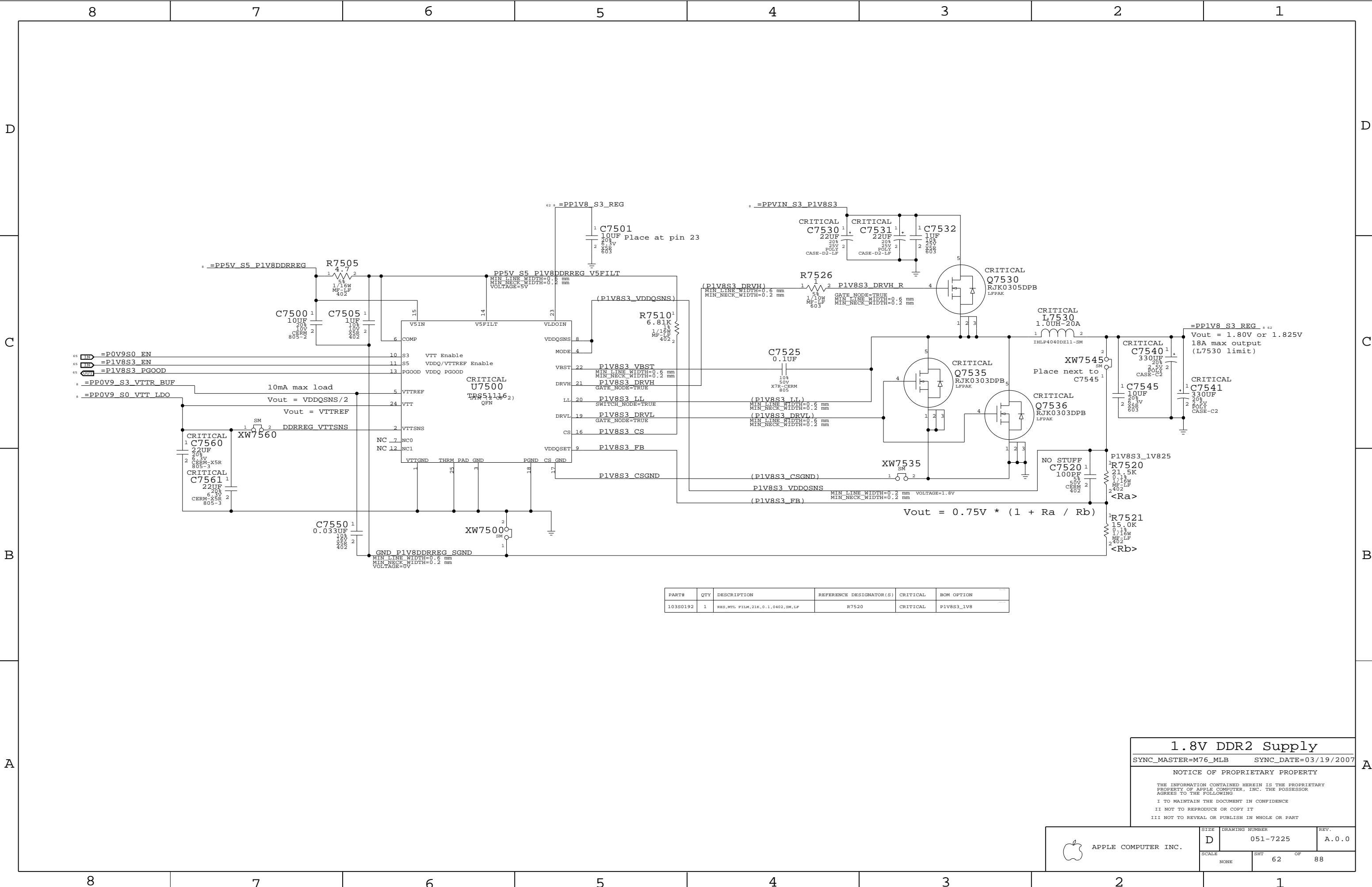
II NOT TO REPRODUCE OR COPY IT

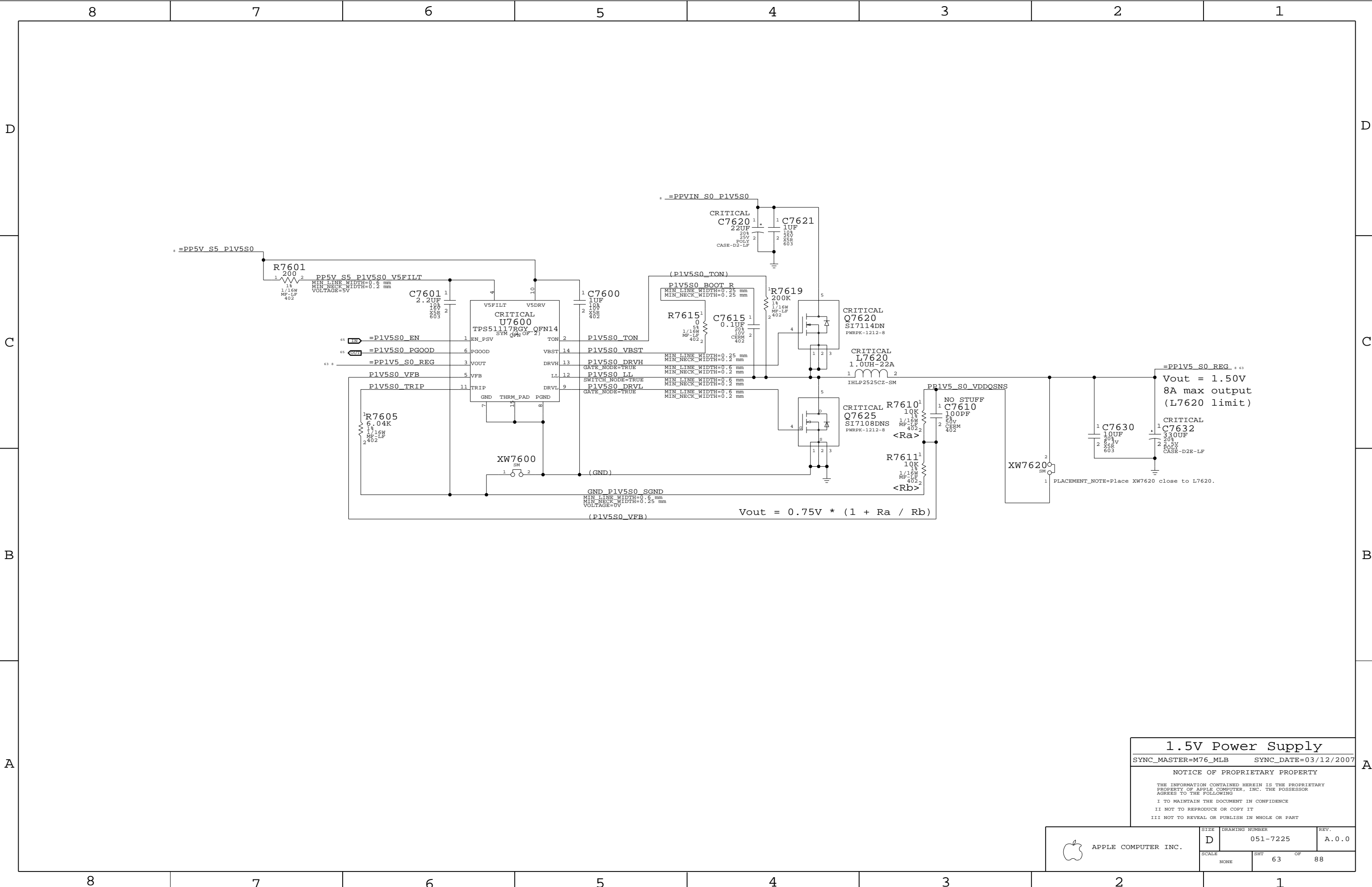
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	61	88





1.5V Power Supply

SYNC_MASTER=M76_MLB

SYNC_DATE=03/12/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

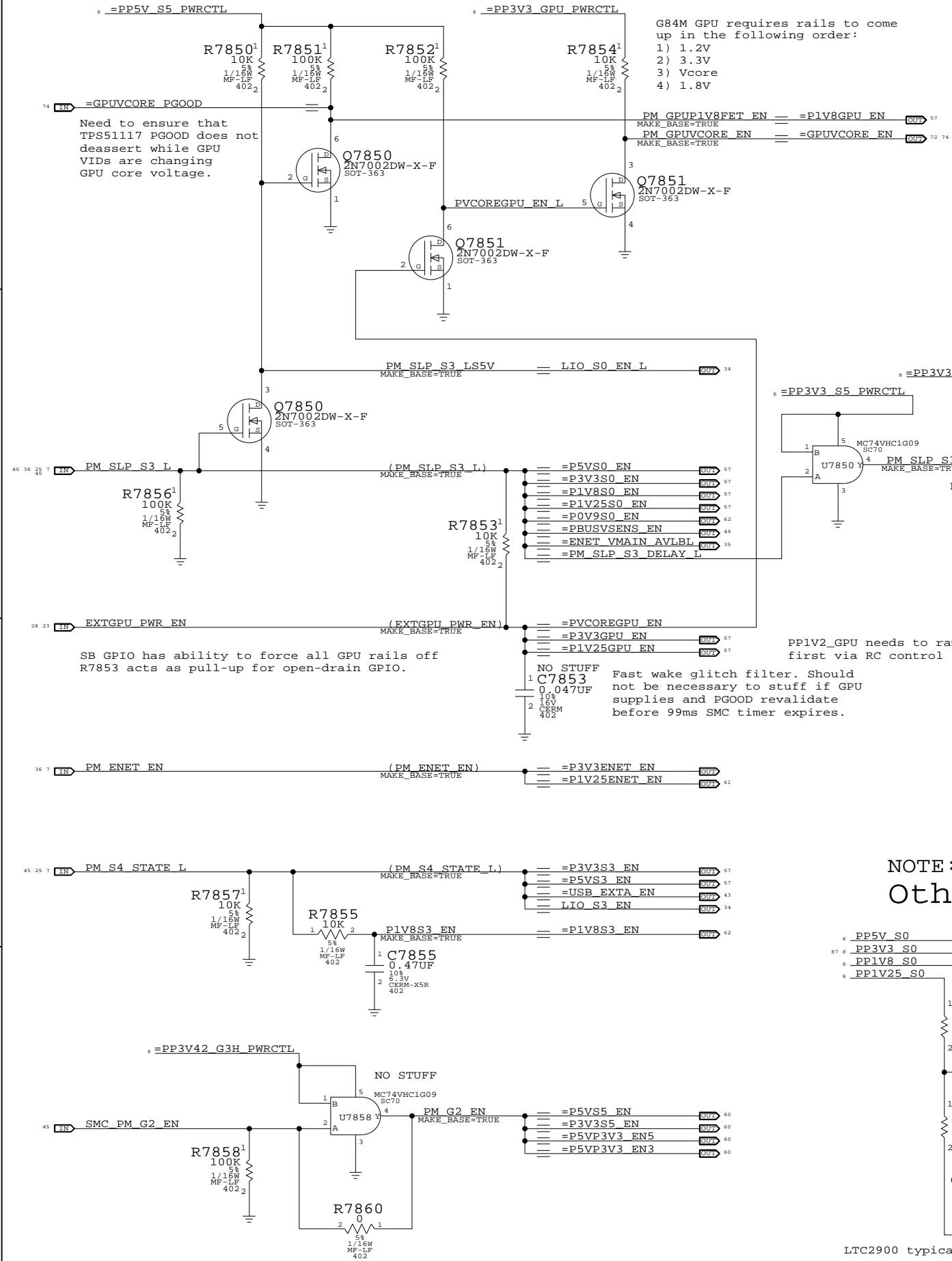
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

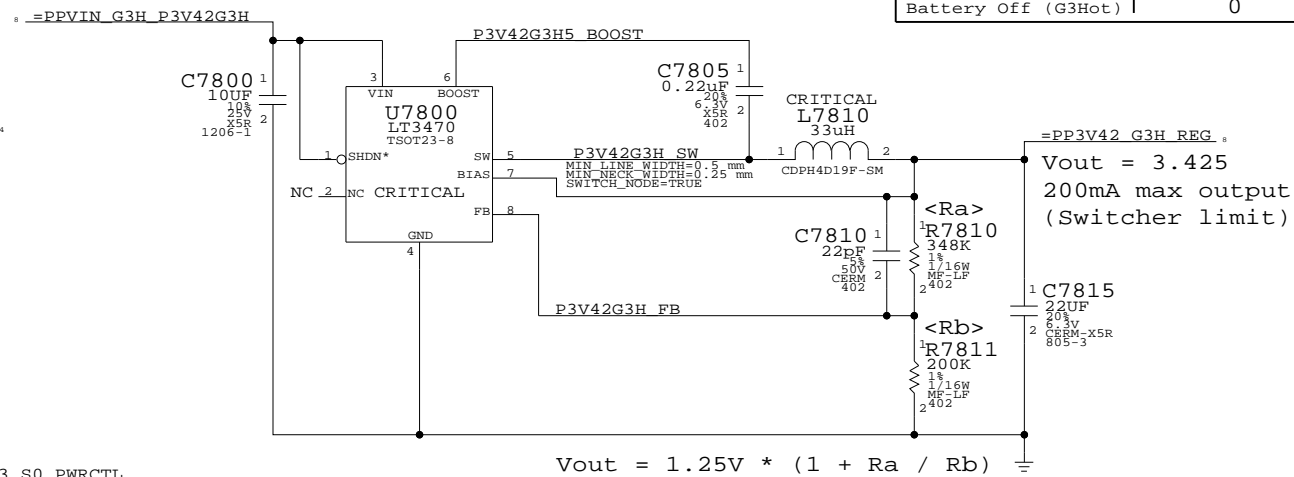
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		63	88

Power Control Signals



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

- Vout = 3.425
200mA max output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b) =$$

Unused PGOOD Signals

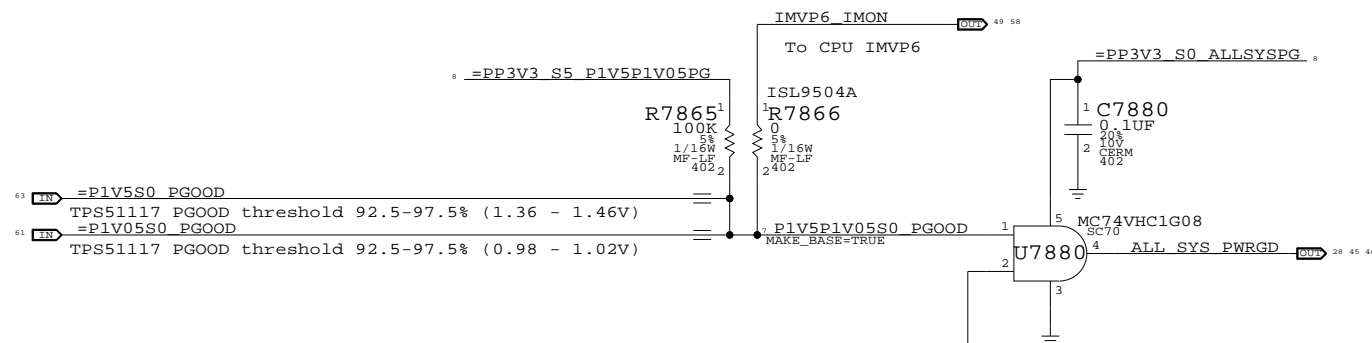
```

61  =P1v25ENET_PGOOD  == TP_P1v25ENET_PGOOD
    == MAKE_BASE=TRUE
62  =P1v8S3_PGOOD     == TP_P1v8S3_PGOOD
    == MAKE_BASE=TRUE

```

1.5V / 1.05V PWRGD Circuit

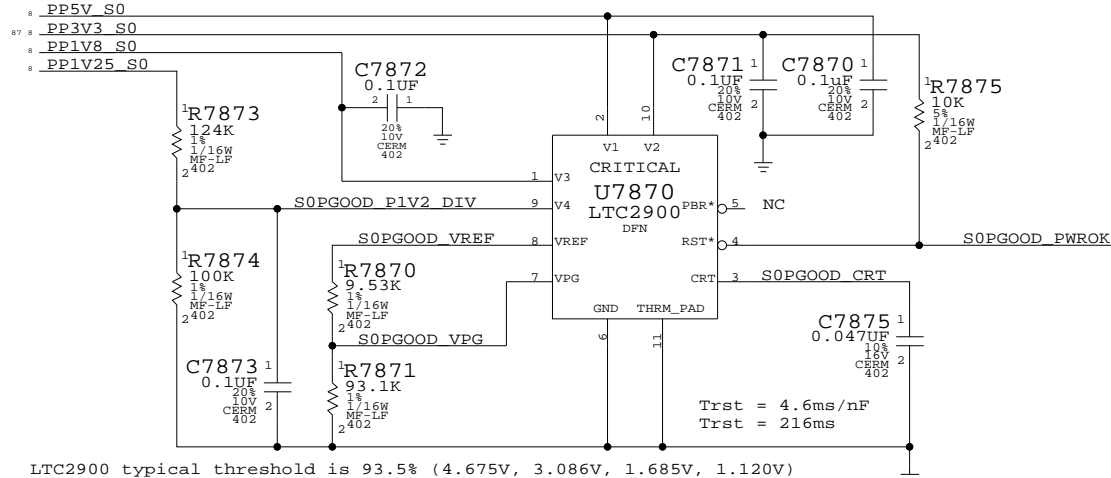
Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include GFX rails



LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
-----------------------	---------------------

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
SCALE NONE	SHT 65	OF 88

```
Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
```

```
Signal aliases required by this page:
(NONE)
```

```
BOM options provided by this page:
(NONE)
```



 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
	SCALE	SHT	OF
	NONE	66	88



APPLE COMPUTER INC.

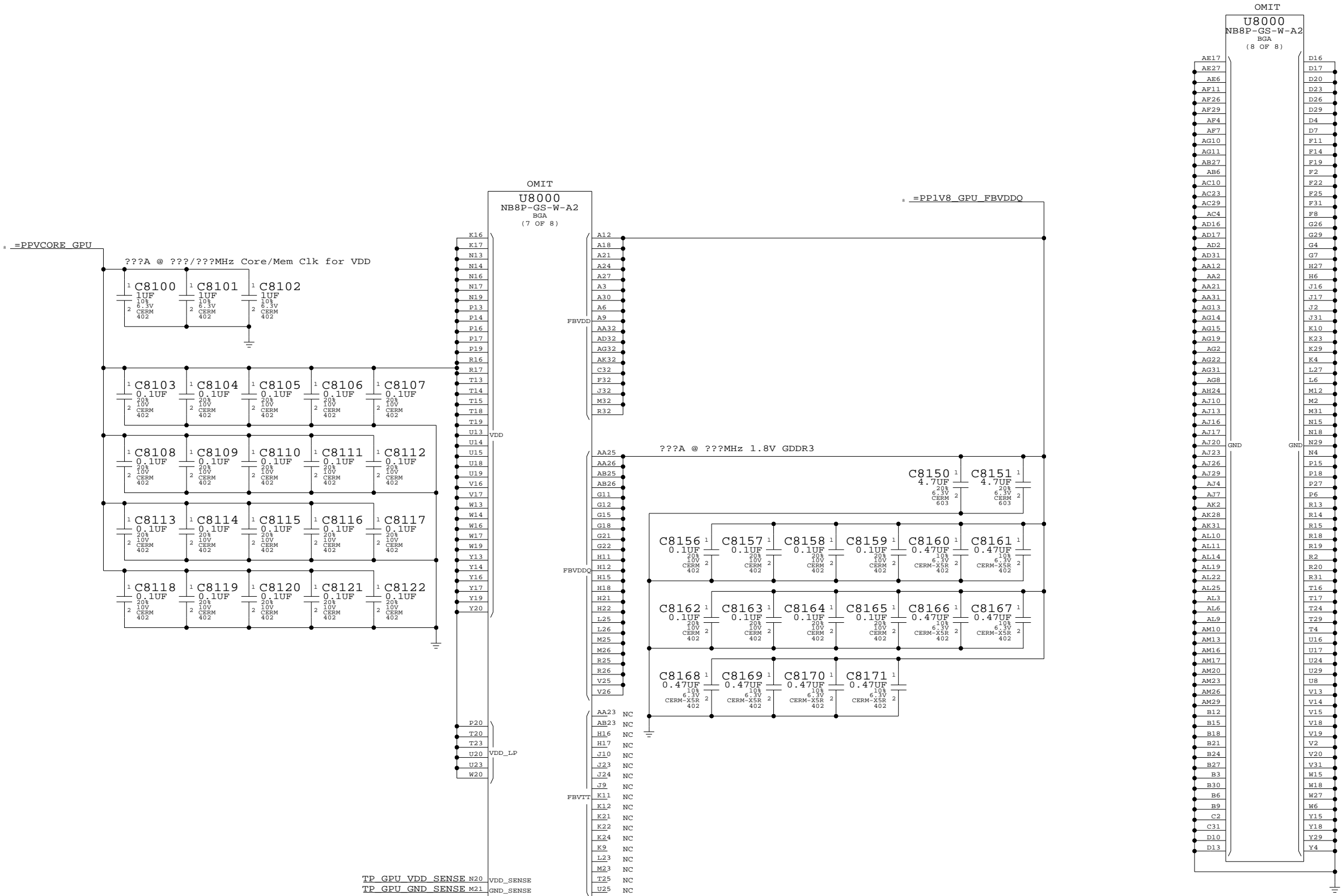
SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
SCALE NONE	SHT 66	OF 88

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

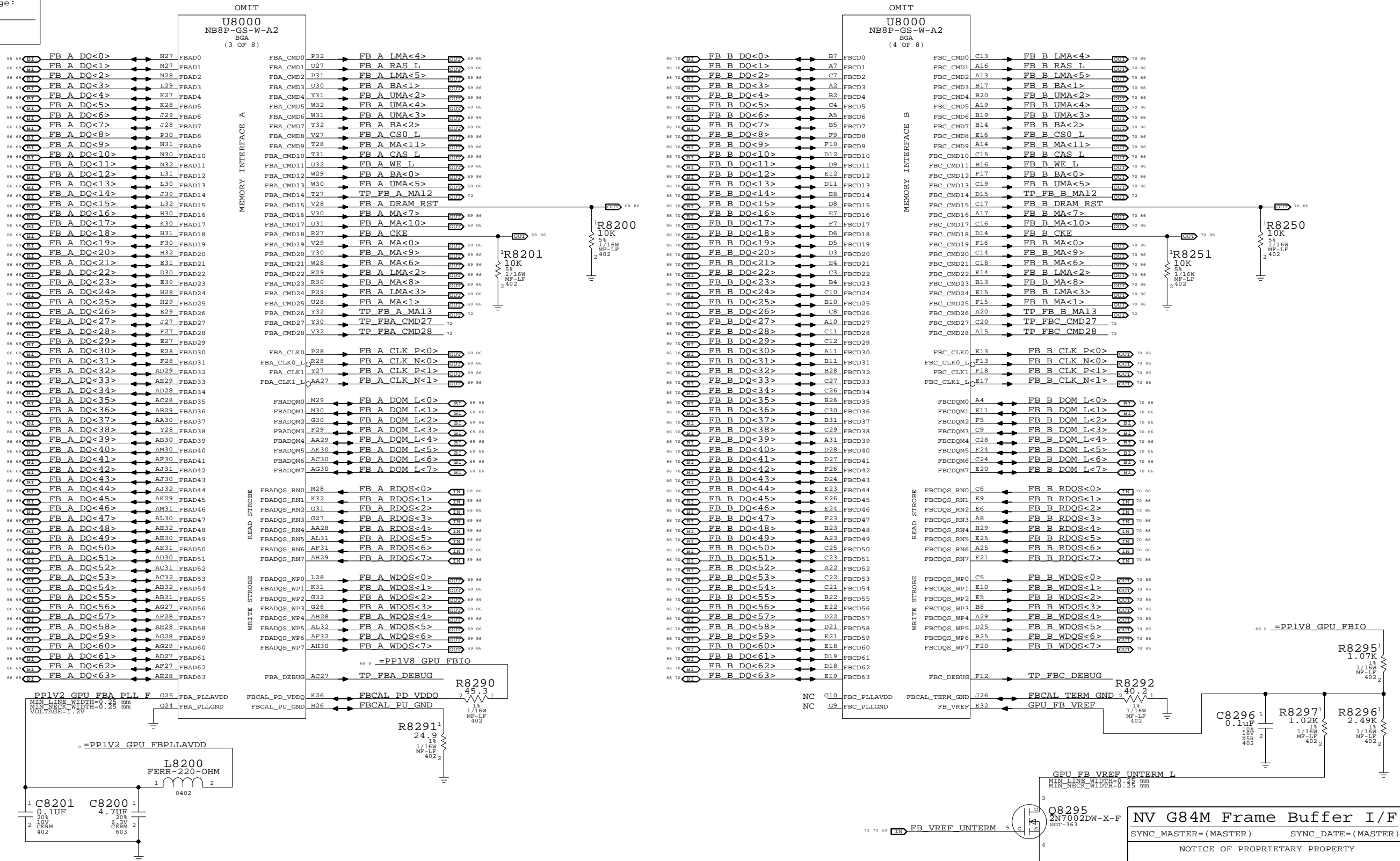
SCALE NONE SHT 67 OF 88

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

SCALE NONE SHT 68 OF 88

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

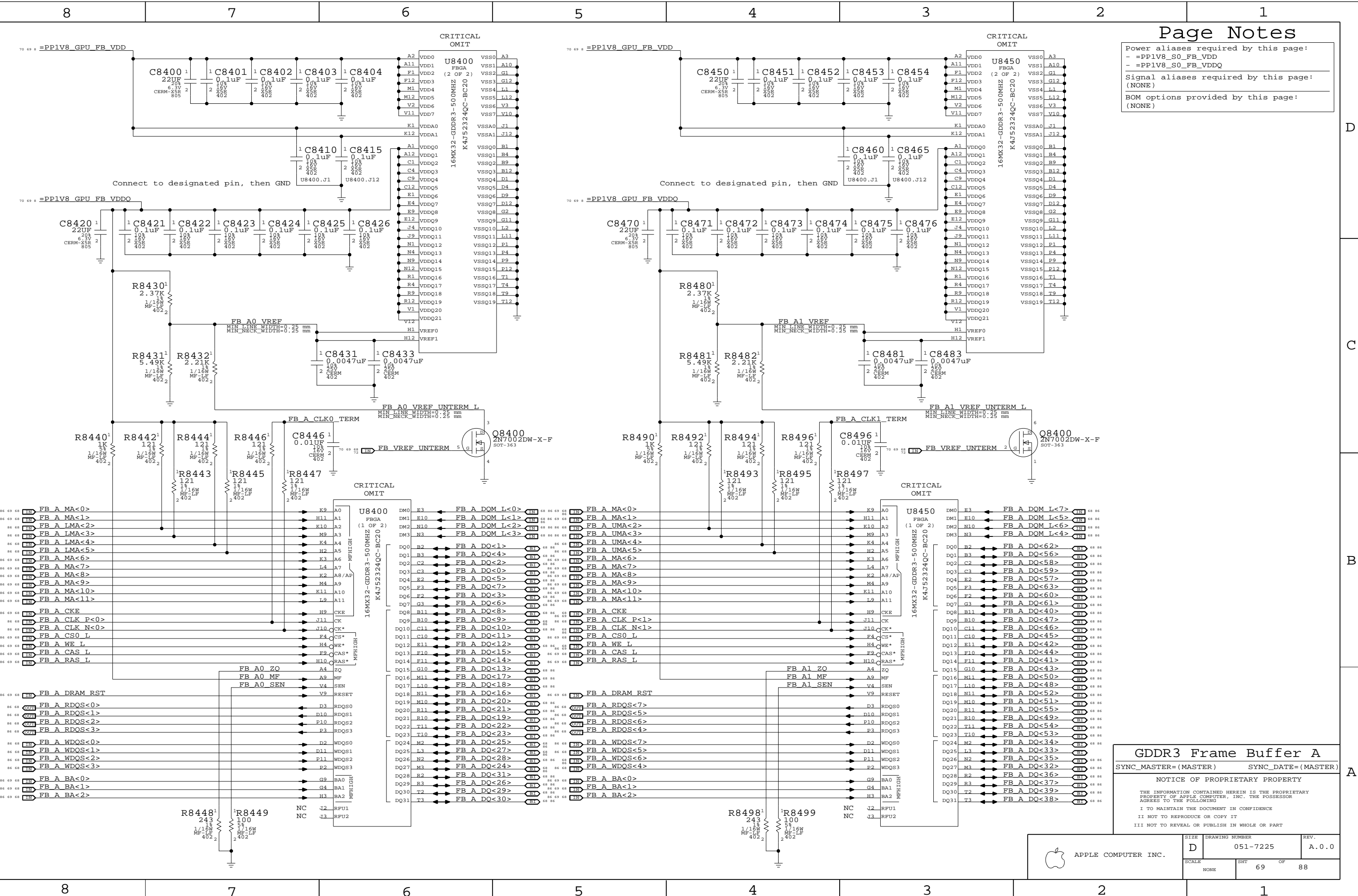
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

SCALE NONE SHT 69 OF 88



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

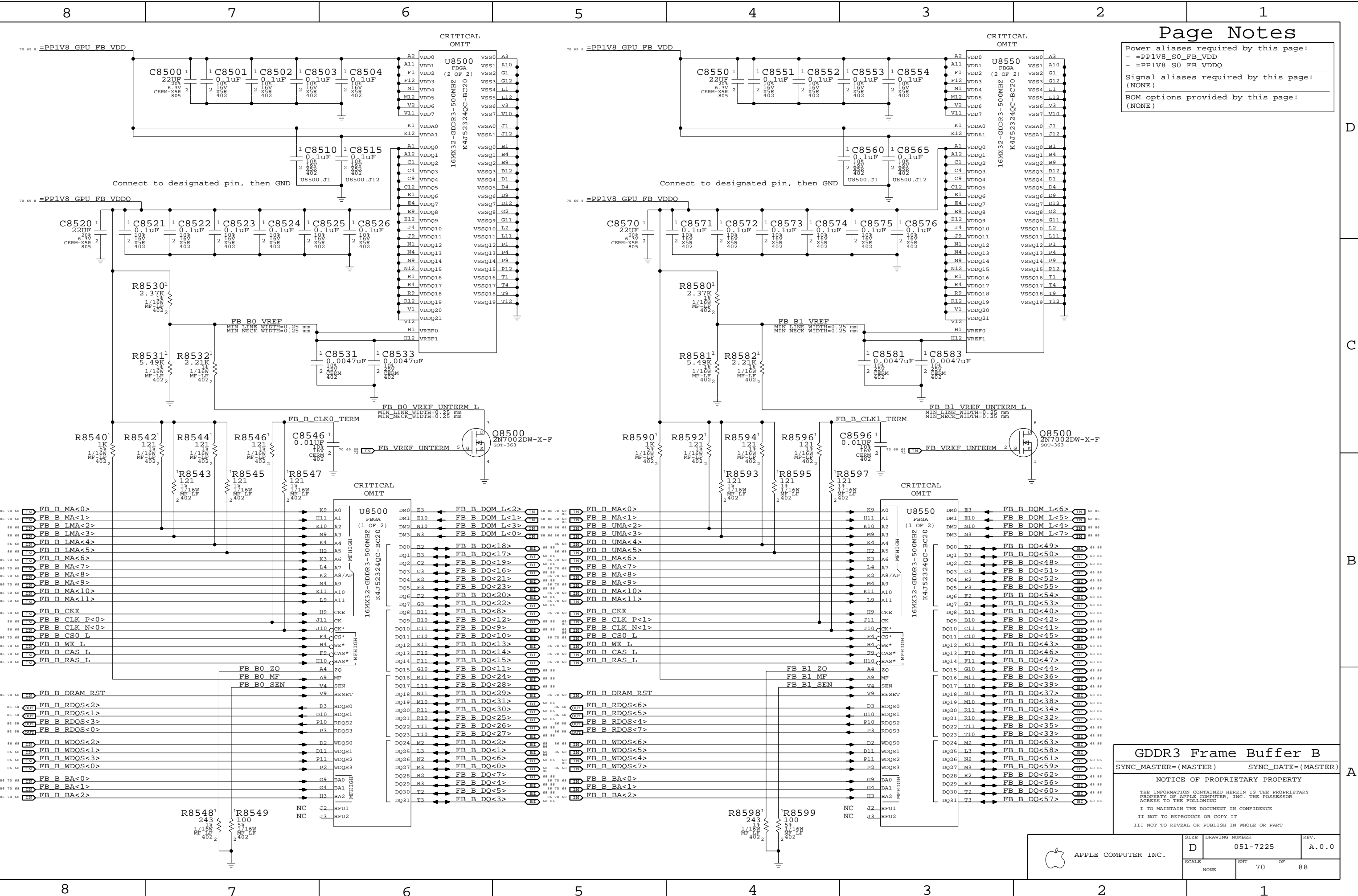
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

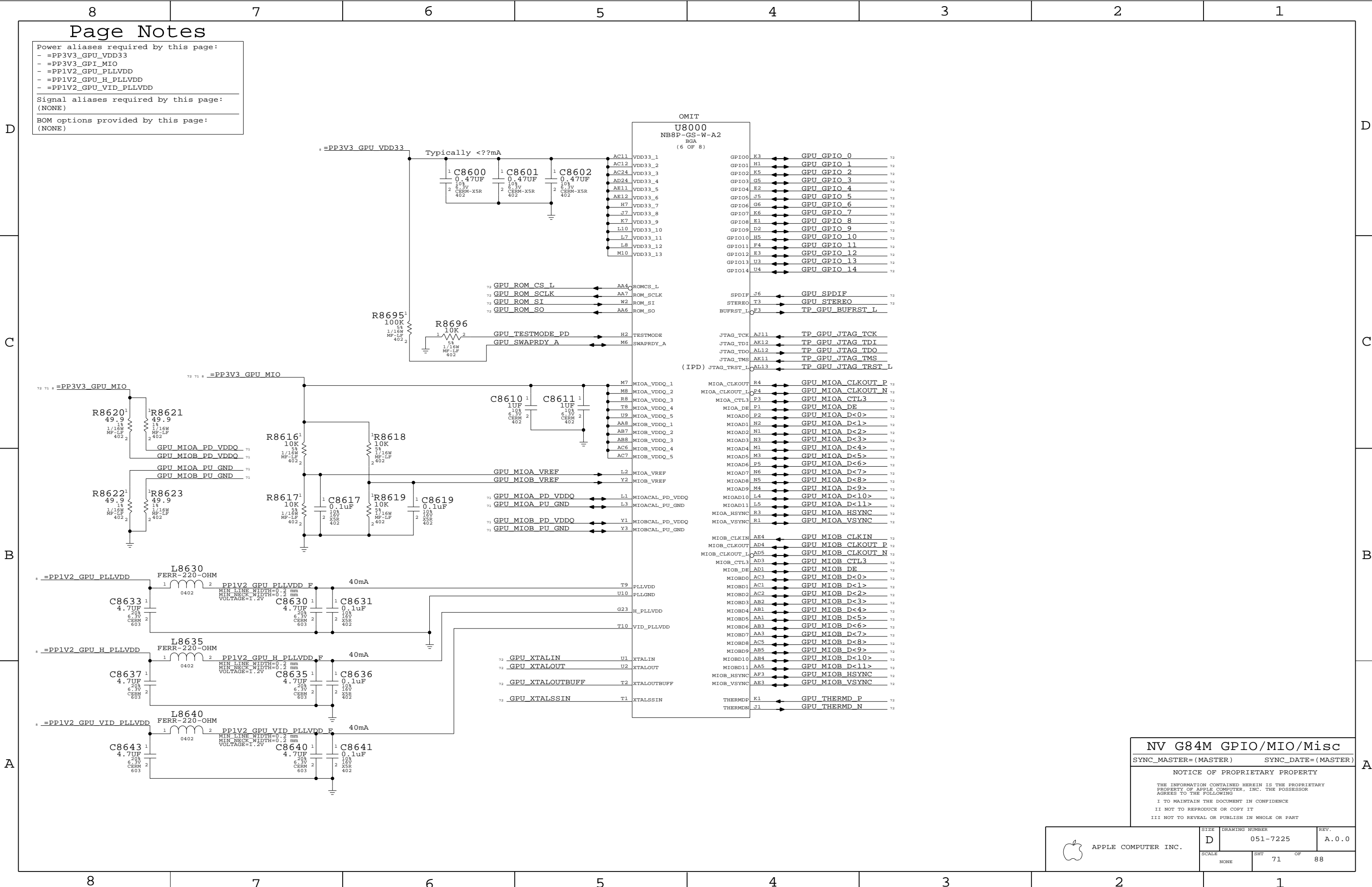


APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

SCALE NONE SHT 70 OF 88





Page Notes

Power aliases required by this page:

- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

=PP1V8_GPU_IFPX

L8800
FERR-220-OHM
0402

20mA peak per diff pair
160mA peak for all pairs

C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402

Place at AF9 Place at AF8

L8805
FERR-220-OHM
0402

40mA peak

C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402

=PP3V3_GPU_IFPCD_IOVDD

L8810
FERR-220-OHM
0402

20mA peak per diff pair
200mA peak for all pairs

C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402

Place at AD6 Place at AE7

L8815
FERR-220-OHM
0402

40mA peak

C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402

Sum of peak currents: 390mA

=PP3V3_GPU_DAC

L8820
FERR-220-OHM
0402

120mA peak

C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402

L8830
FERR-220-OHM
0402

150mA peak

C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402

NO STUFF

L8840
FERR-220-OHM
0402

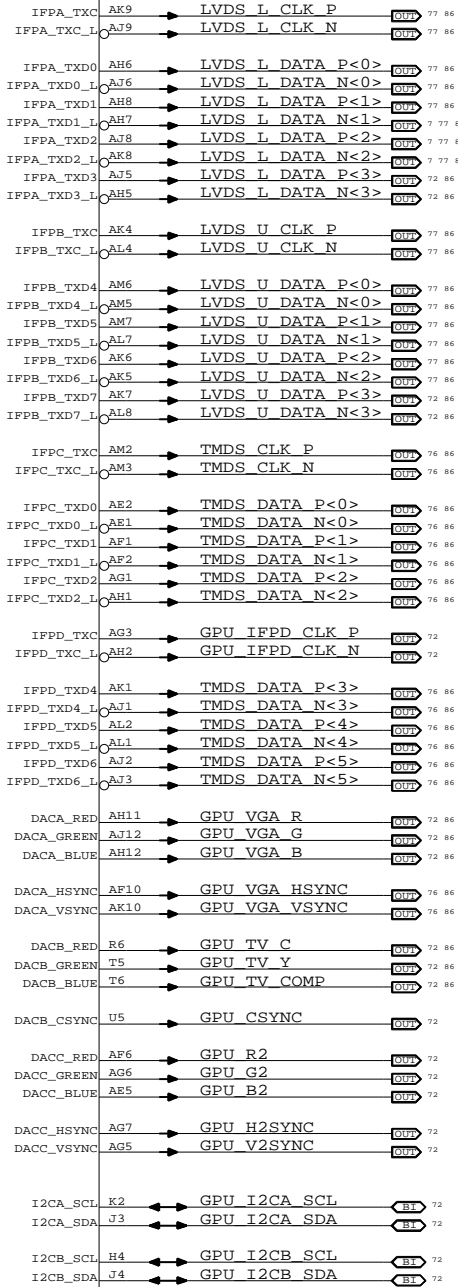
120mA peak

C8845 4.7UF 20% 6.3V CERM 603
C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT

U8000
NB8P-GS-W-A2
BGA
(5 OF 8)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

NV G84M Video Interfaces

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

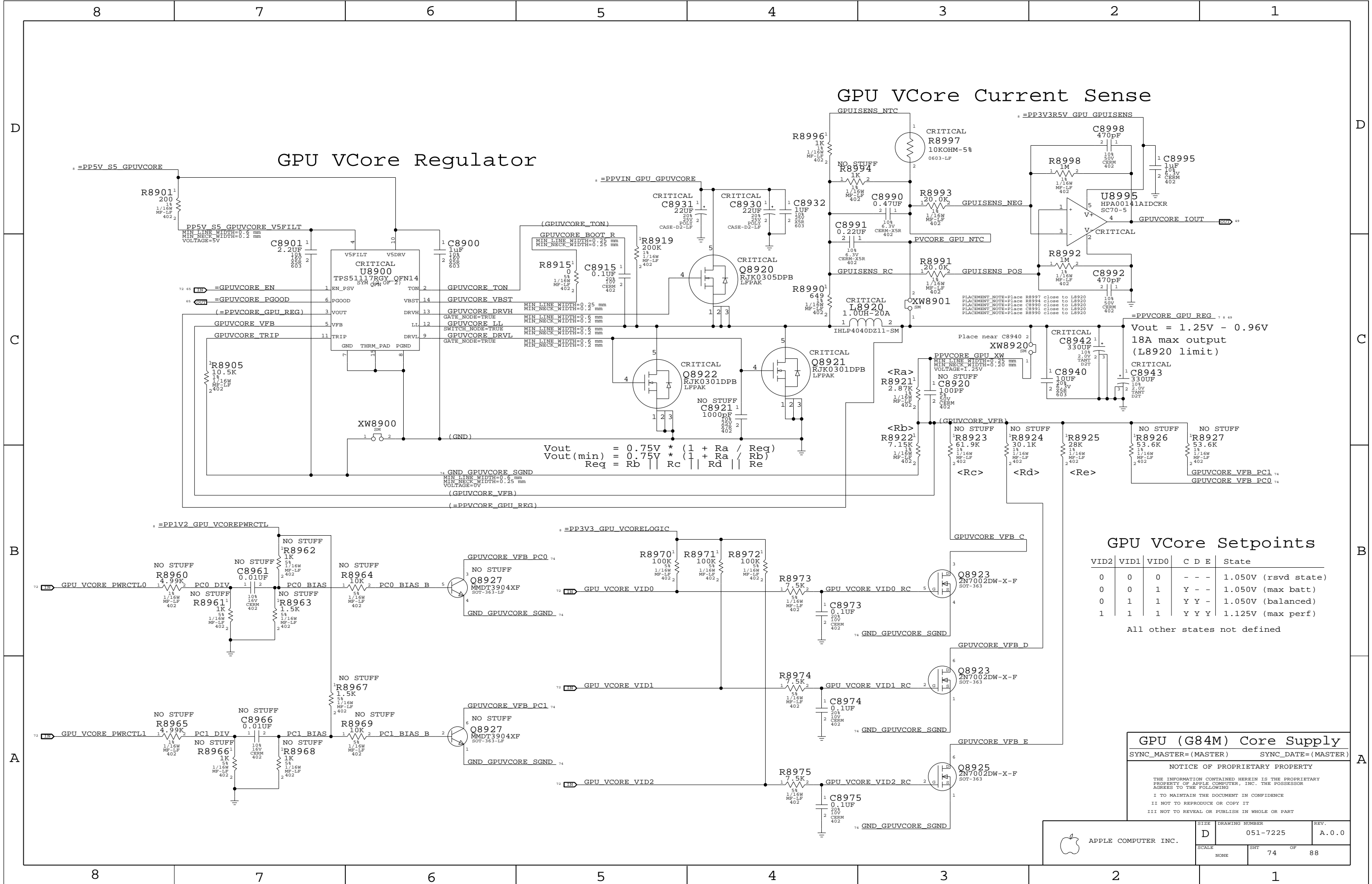
II NOT TO REPRODUCE OR COPY IT

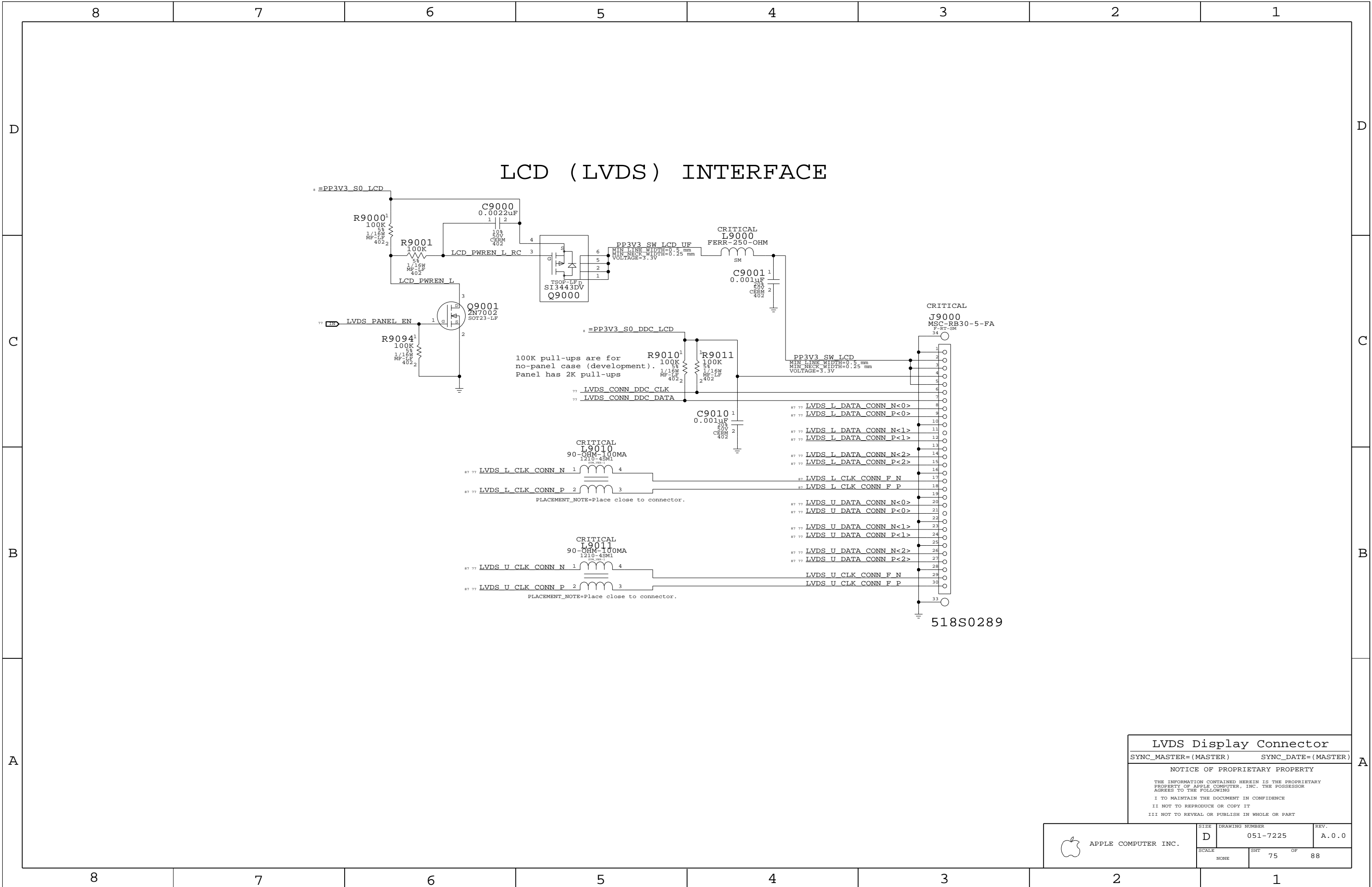
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	73	88





LVD

S

Display Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

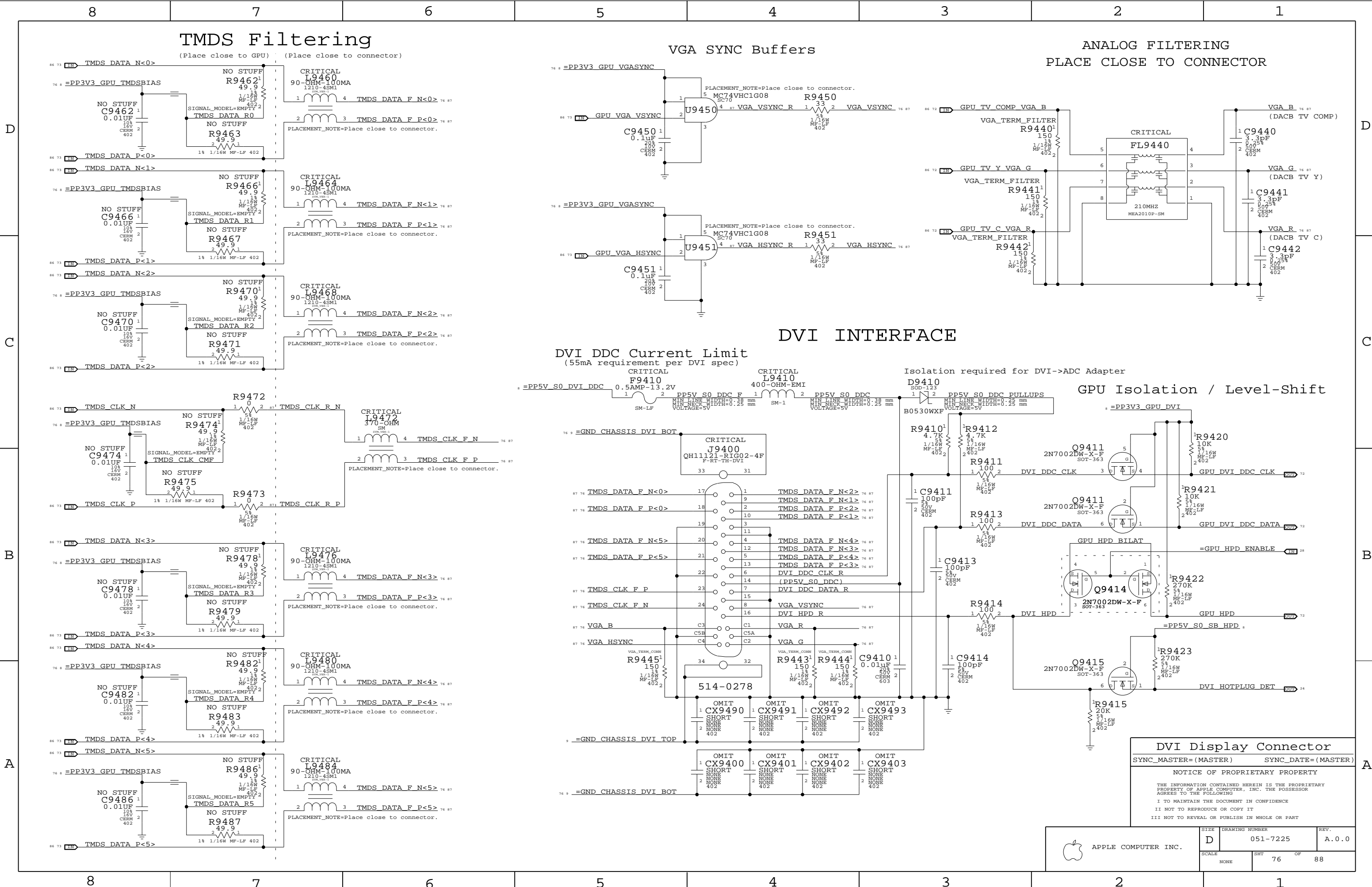
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		75	88



TMDS Filtering

(Place close to GPU) (Place close to connector)

VGA SYNC Buffers

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

DVI INTERFACE

DVI DDC Current Limit (55mA requirement per DVI spec)

GPU Isolation / Level-Shift

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

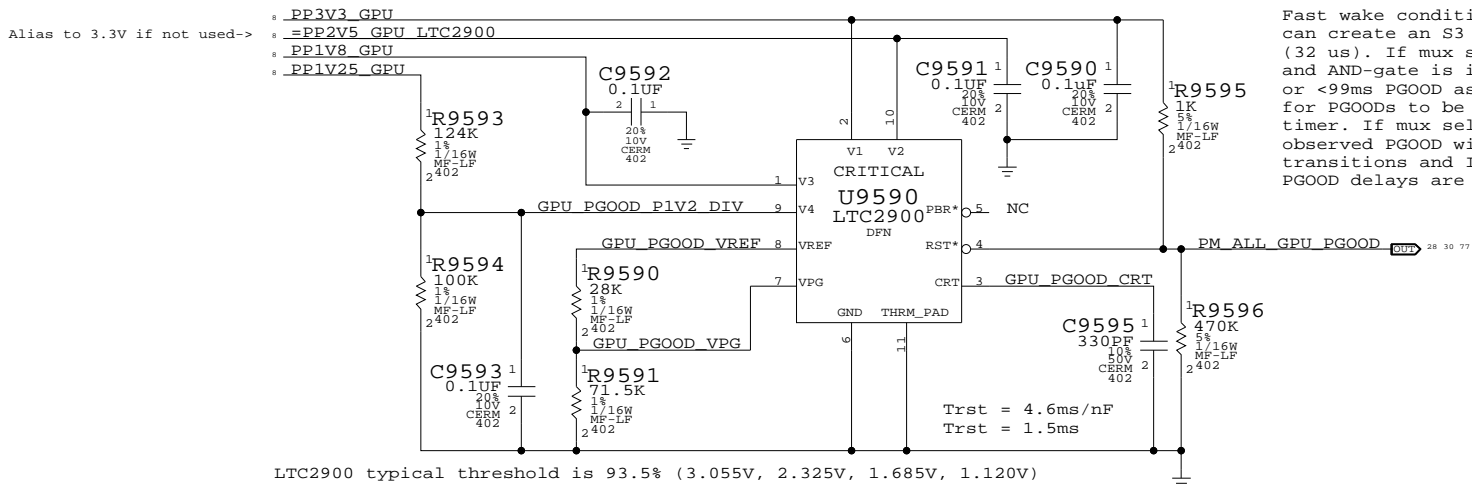
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

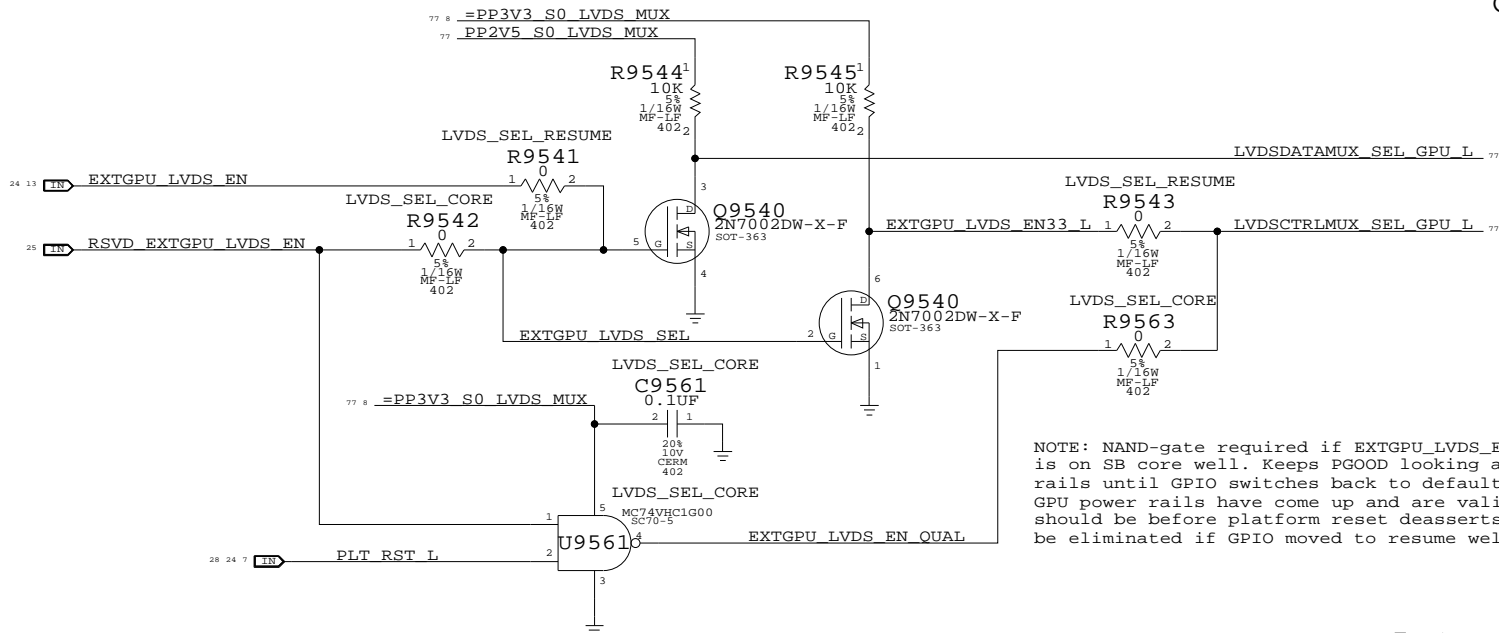
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 76	OF 88

PGOOD Monitor for GPU Rails

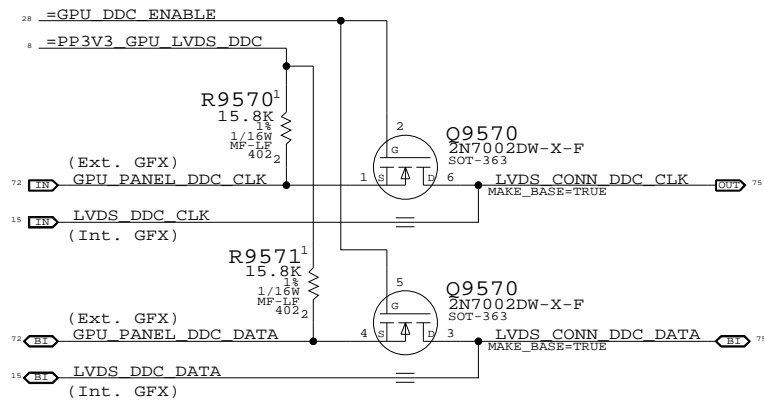
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



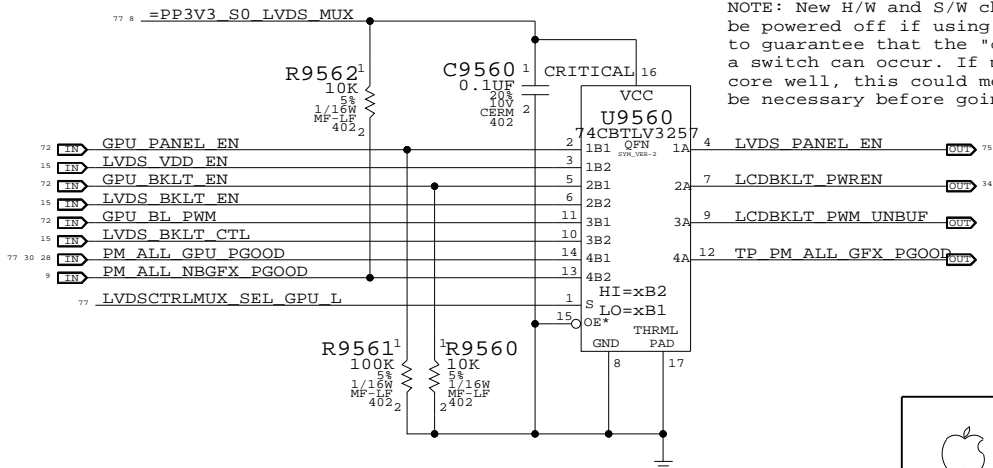
Mux Select Conditioning



GPU DDC Pass FETs

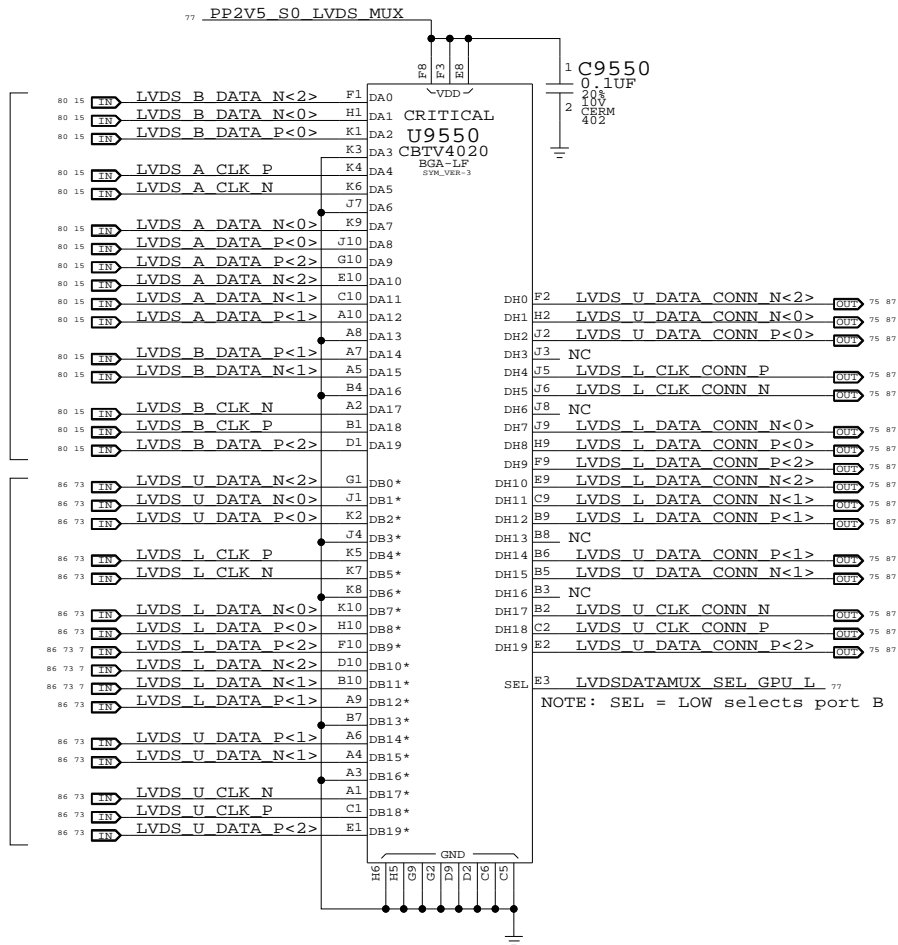


Panel/Backlight Control Mux

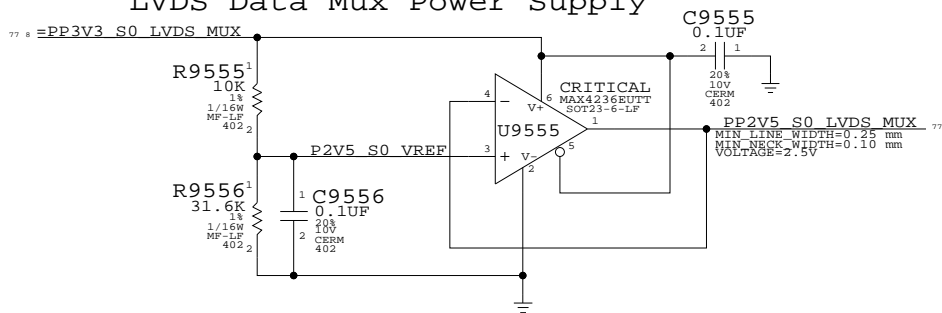


NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

LVDS I/F Mux



LVDS Data Mux Power Supply



LVDS Interface Mux

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

DRAWING NUMBER

REV.

D

051-7225

A.0.0

SCALE

NONE

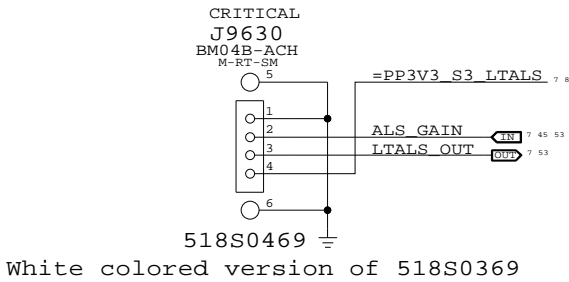
SHT

77

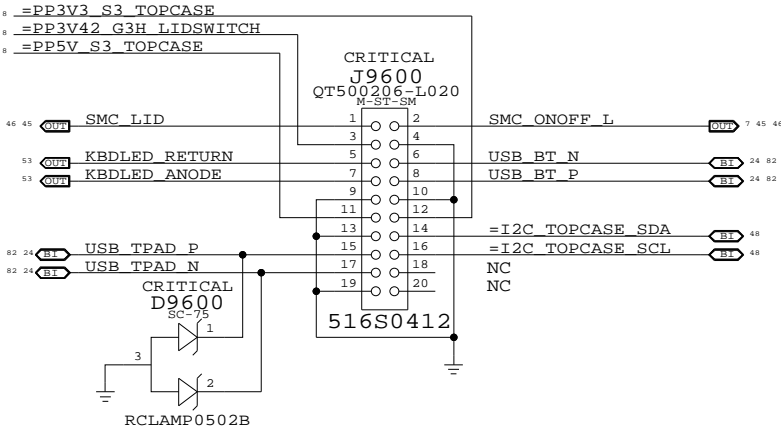
OF

88

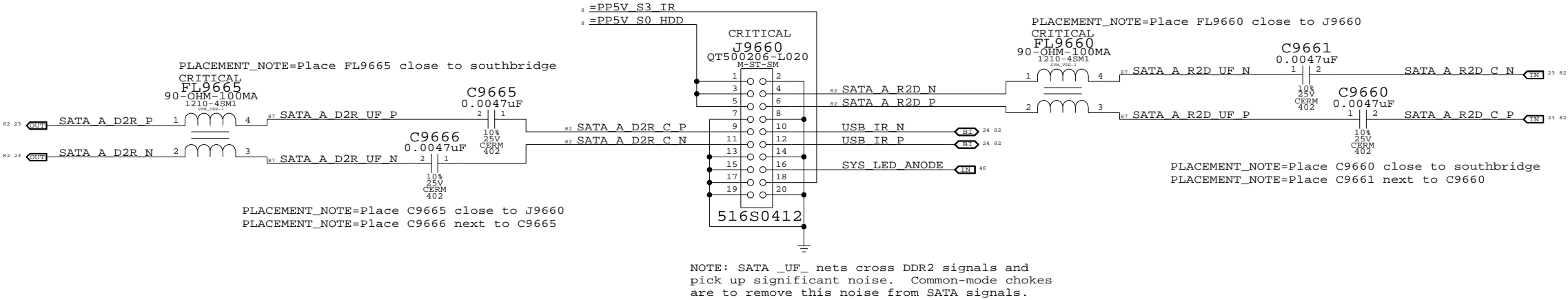
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7225

REV.

A.0.0

SHT

78

OF

88

8

7

6

5

4

3

2

1

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>	66
	PCIE_100D	PCIE	PEG R2D N<15..0>	66
	PCIE_100D	PCIE	PEG R2D_C P<15..0>	15 66
	PCIE_100D	PCIE	PEG R2D_C_N<15..0>	15 66
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>	15 66
	PCIE_100D	PCIE	PEG D2R N<15..0>	15 66
	PCIE_100D	PCIE	PEG D2R_C P<15..0>	66
	PCIE_100D	PCIE	PEG D2R_C_N<15..0>	66
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	16 24
	DMI_100D	DMI	DMI N2S N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	16 24
	DMI_100D	DMI	DMI S2N N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P	15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>	15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>	
LVDS_IBG		LVDS	LVDS IBG	15 22
CRT_TVO_IREF		CRT	CRT TVO IREF	
CRT_RED	CRT_50S	CRT	CRT RED	
CRT_GREEN	CRT_50S	CRT	CRT GREEN	
CRT_BLUE	CRT_50S	CRT	CRT BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	

8

7

6

5

4

3

2

1

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	80	88

8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

SCALE NONE SHT 81 OF 88

8

7

6

5

4

3

2

1

Disk Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L	23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L	23 42
IDE_CNTRL	IDE_55S	IDE	IDE_PDIOW L	23 42
IDE_PDIOIR_L	IDE_55S	IDE	IDE_PDIOIR L	23 42
IDE_CNTRL	IDE_55S	IDE	IDE_PDDACK L	23 42
IDE_CNTRL	IDE_55S	IDE	IDE_PDDREQ	23 42
IDE_PDIOIRDY	IDE_55S	IDE	IDE_PDIOIRDY	23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L	24 42
SATA_A_R2D	SATA_100D	SATA	SATA A R2D C P	23 78
	SATA_100D	SATA	SATA A R2D C N	23 78
	SATA_100D	SATA	SATA A R2D P	78
	SATA_100D	SATA	SATA A R2D N	78
SATA_A_D2R	SATA_100D	SATA	SATA A D2R P	23 78
	SATA_100D	SATA	SATA A D2R N	23 78
	SATA_100D	SATA	SATA A D2R C P	78
	SATA_100D	SATA	SATA A D2R C N	78
SATA_B_R2D	SATA_100D	SATA	SATA B R2D C P	23 42
	SATA_100D	SATA	SATA B R2D C N	23 42
	SATA_100D	SATA	SATA B R2D P	
	SATA_100D	SATA	SATA B R2D N	
SATA_B_D2R	SATA_100D	SATA	SATA B D2R P	23 42
	SATA_100D	SATA	SATA B D2R N	23 42
	SATA_100D	SATA	SATA B D2R C P	
	SATA_100D	SATA	SATA B D2R C N	
SATA_C_R2D	SATA_100D	SATA	SATA C R2D C P	23 42
	SATA_100D	SATA	SATA C R2D C N	23 42
	SATA_100D	SATA	SATA C R2D P	
	SATA_100D	SATA	SATA C R2D N	
SATA_C_D2R	SATA_100D	SATA	SATA C D2R P	23 42
	SATA_100D	SATA	SATA C D2R N	23 42
	SATA_100D	SATA	SATA C D2R C P	
	SATA_100D	SATA	SATA C D2R C N	
SATA_RBIAS	SATA_55S		SATA RBIAS	42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT_CLK	23 34
	HDA_55S	HDA	HDA BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 34
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 34
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23
	HDA_55S	HDA	HDA_SDIN_CODECC	
HDA_SDOUIT	HDA_55S	HDA	HDA_SDOUIT	23 34
	HDA_55S	HDA	HDA_SDOUIT_R	
USB_EXT_A	USB_90D	USB	USB_EXT_A_P	24 43
	USB_90D	USB	USB_EXT_A_N	24 43
	USB_90D	USB	USB_EXT_A_MUXED_P	
	USB_90D	USB	USB_EXT_A_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
USB_EXTD	USB_90D	USB	USB_EXTD_P	24 44
	USB_90D	USB	USB_EXTD_N	24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24
	USB_90D	USB	USB_CAMERA_N	7 24
USB_BT	USB_90D	USB	USB_BT_P	24 78
	USB_90D	USB	USB_BT_N	24 78
USB_TPAD	USB_90D	USB	USB_TPAD_P	24 78
	USB_90D	USB	USB_TPAD_N	24
USB_IR	USB_90D	USB	USB_IR_P	24 78
	USB_90D	USB	USB_IR_N	24 78
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 34
	USB_90D	USB	USB_EXTB_N	24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	24 34
	USB_90D	USB	USB_EXCARD_N	24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 34
	USB_90D	USB	USB_EXTC_N	9 34
USB_RBIAS	USB_60S		USB RBIAS	24
SMB_SB_SCI	SMB_55S	SMB	SMB_CLK	25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 48
SMB_MB_SF_SCI	SMB_55S	SMB	SMB_ME_CLK	25 48
SMB_MB_SF_SDA	SMB_55S	SMB	SMB_ME_DATA	25 48
SPI_SCL_K	SPI_55S	SPI	SPI_SCL_K_R	24 55
	SPI_55S	SPI	SPI_SCL_K	55
	SPI_55S	SPI	SPI_A_SCL_K_R	
	SPI_55S	SPI	SPI_B_SCL_K_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 55
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	55
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	24 55
	SPI_55S	SPI	SPI_A_SO_R	55
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_I_0	SPI_55S	SPI	SPI_CE_R_L<0>	24 55
	SPI_55S	SPI	SPI_CE_L<0>	55
SPI_CE_I_1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007	7
---------------------	----------------------	---


NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
	SCALE	SHT OF	
	NONE	82	88

8

7

6

5

4

3

2

1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
<div></div>	CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P		29 30
<div></div>	CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N		29 30
<div></div>	CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P		29 30
<div></div>	CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N		29 30
<div></div>	CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P		29 30
<div></div>	CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N		29 30
<div></div>	CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0_CLK_ITREN		29 30
<div></div>	CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK		29 30
<div></div>	CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK		29 30
<div></div>	CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK		29 30
<div></div>	CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK		29 30
<div></div>	CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK		29 30
<div></div>	CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL		29 30
<div></div>	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA		29 30
<div></div>	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC		29 30
<div></div>	CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P		29 30
<div></div>	CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N		29 30
<div></div>	CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P		29 30
<div></div>	CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N		29 30
<div></div>	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P		29 30
<div></div>	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N		29 30
<div></div>	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P		29 30
<div></div>	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N		29 30
<div></div>	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P		29 30
<div></div>	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N		29 30
<div></div>	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P		29 30
<div></div>	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N		29 30
<div></div>	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P		29 30
<div></div>	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N		29 30
<div></div>	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P		29 30
<div></div>	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N		29 30
<div></div>	CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P		29 30
<div></div>	CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N		29 30
<div></div>	CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P		29 30
<div></div>	CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N		29 30
<div></div>	(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P		10 30
<div></div>	(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N		10 30
<div></div>	(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P		7 14 30
<div></div>	(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N		7 14 30
<div></div>	(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P		13 30 79
<div></div>	(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N		13 30 79
<div></div>	(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS		7 30 47
<div></div>	(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB		24 30
<div></div>	(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW		30 38
<div></div>	(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM		
<div></div>	(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC		30 45
<div></div>	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_PCI4 is project-specific		
<div></div>	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_PCI5 is project-specific		
<div></div>	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR		25 30
<div></div>	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER		25 30
<div></div>	(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	CK505_FSA		30
<div></div>	(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	CK505_FSC		30
<div></div>	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P		7
<div></div>	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N		7
<div></div>	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P		7 22 30
<div></div>	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N		7 22 30
<div></div>	(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P		9
<div></div>	(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N		9
<div></div>	(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P		24 30
<div></div>	(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N		24 30
<div></div>	(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P		30 34
<div></div>	(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N		30 34
<div></div>	(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P		23 30
<div></div>	(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N		23 30
<div></div>	(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P		7 16 30
<div></div>	(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N		7 16 30
<div></div>	(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P		30 34
<div></div>	(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N		30 34
<div></div>	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 is project-specific		
<div></div>	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P		30 35
<div></div>	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N		30 35

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		PHYSICAL	SPACING	
<div></div>	SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL		48
<div></div>	SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA		48
<div></div>	SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL		48
<div></div>	SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA		48
<div></div>	SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL		48
<div></div>	SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA		48
<div></div>	SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL		48
<div></div>	SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA		48
<div></div>	SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL		48
<div></div>	SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA		48

Clock & SMC Constraints

SYNC_MASTER=T9_NONE SYNC_DATE=01/17/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

8

7

6

5

4

3

2

1

APPLE COMPUTER INC.

D

051-7225

A.0.0

SCALE

NONE

SMT

84

OF

88

87654321

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW LINK<7..0>
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW CTL<1..0>
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON_R
<input type="checkbox"/> FW_LPS	FW_55S	FW	FW LPS 38 39
<input type="checkbox"/> FW_LREQ	FW_55S	FW	FW LREQ 38 39
<input type="checkbox"/> FW_PINT	FW_55S	FW	FW PINT 38 39
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P 39 41
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N 39 41
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P 39 41
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N 39 41
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P 39 41
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N 39 41
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P 39 41
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N 39 41
Port 2 Not Used			

87654321

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007


NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
SCALE NONE	SHT 85 OF 88	

87654321

[illegible]

<

